

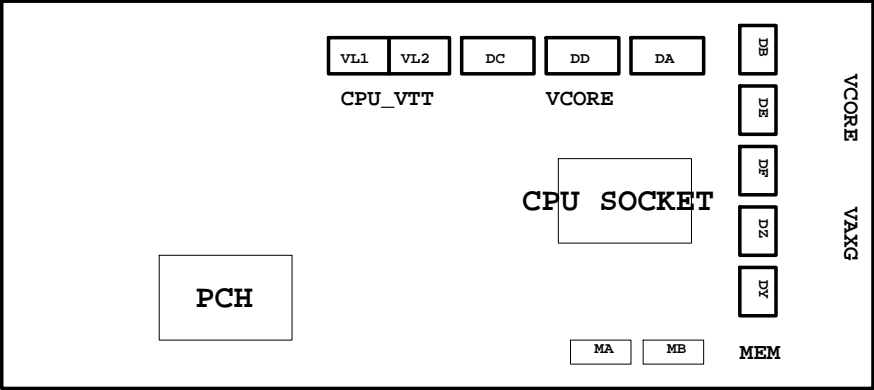
Model Name: GA-Z77X-UP4 TH 1.2

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP_HDMI_DVI_DAC,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*1 SLOTS X3
18	PCI EXPRESS*16/*8/*4 SWITCH
19	IT8892 PCIE to PCI BRIDGE
20	PCI SLOT
21	HDMI / DVI Connector
22	mSATA Connector
23	Dual BIOS , TPM
24	Realtek 892
25	REAR AUDIO JACK
26	VCORE PWM_IR3567A -1
27	VCORE PWM_IR3567A -2

SHEET TITLE

28	DDR_15V & CPUVTT PWM_IR3570-1
29	DDR_15V & CPUVTT PWM_IR3570-2
30	DISCRETE POWER 1
31	DISCRETE POWER 2
32	I/O IT8728F
33	USB3 , KB/USB3, -PHOT
34	F_PANEL , F_USB , F_USB3
35	ATX POWER, CLOCK BUFFER
36	HWM, FAN CTRL
37	REALTEK 8111F
38	PLX PEX8605 PCIE*1 X3
39	OV NCT3933 / COM
40	VIA VL800
41	DP SWITCH
42	CACTUS RIDGE(THUNDERBOLT)
43	mDP -1
44	mDP -2
45	TABLE LIST

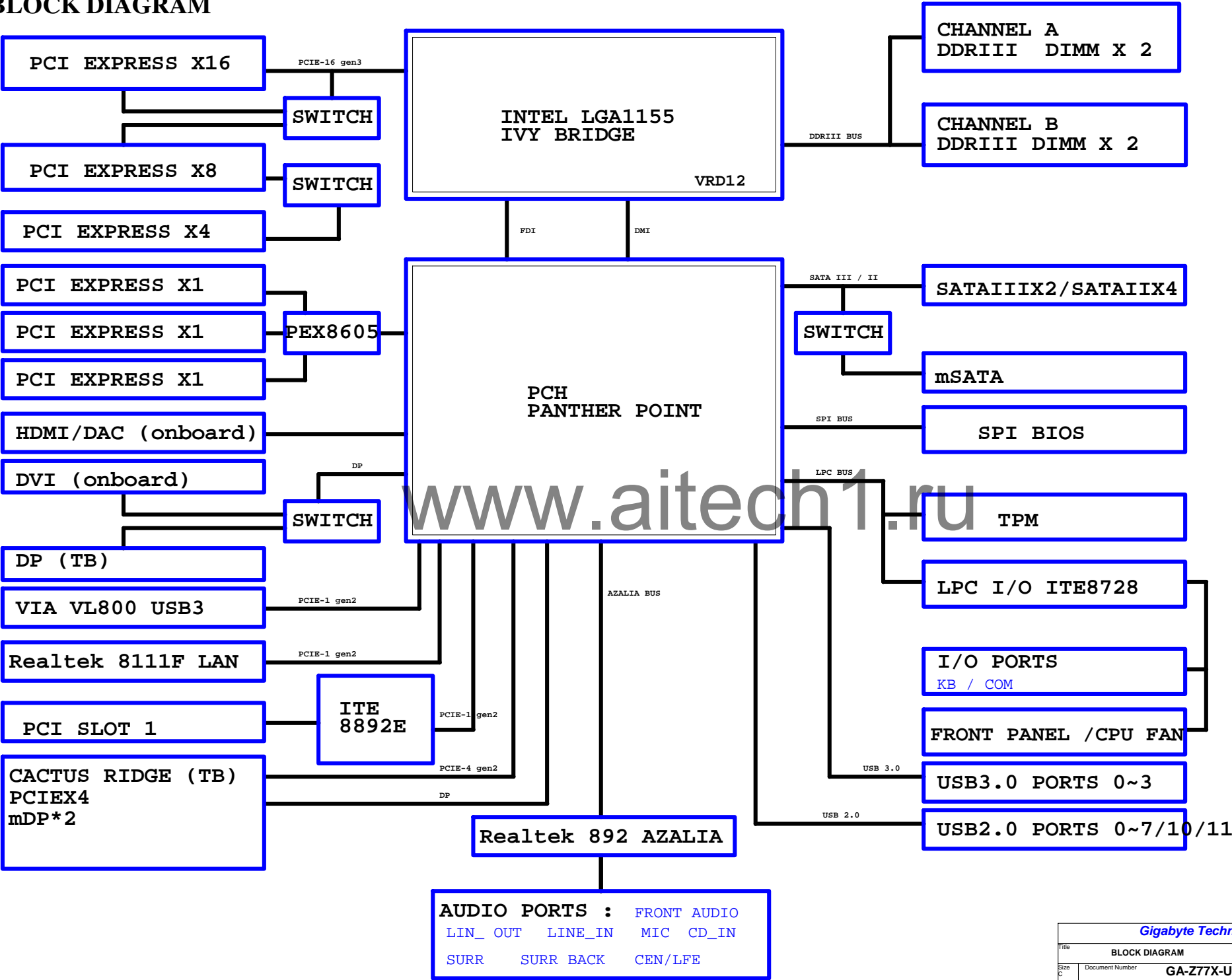


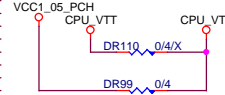
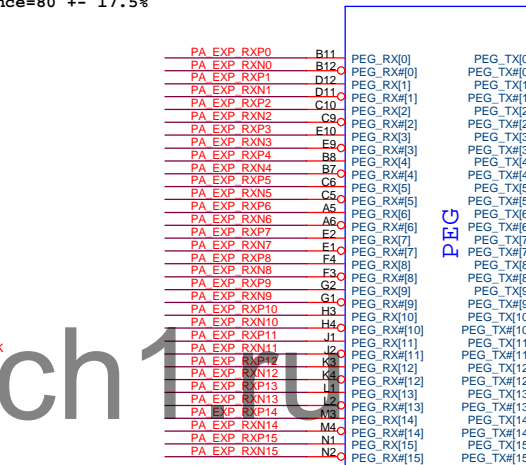
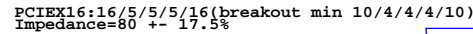
Component value change history

[illegible]

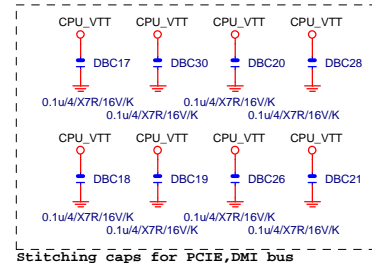
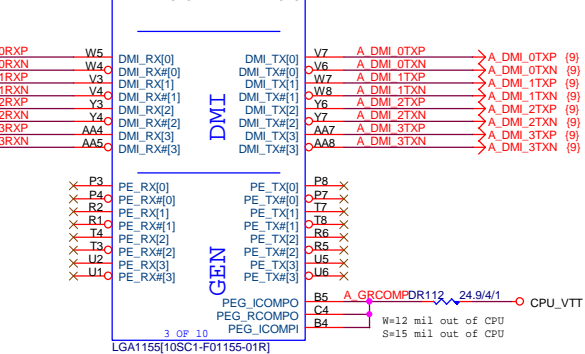
DATE	Change Item	Reason
2012/03/07	0.1 SCH modify from 277X-UD3H VCOORE change PWRSTAGE 3550 11*11 choke + 820uF VTT change 1+1 / 2 phase TB 4C PLX8605 PCIE*1 SW Remove 9172 SATA3 PCIEX16/X8/X4 sharing COM port	Spec Change
2012/03/30	0.2 SCH modify LAN solution change to 8111F Codec soluion change to 892 VAXG Phase2 ISEN/RSEN link SWAP DP/DVI SW SCH modify	
2012/04/06	Add SPDIF_IN	
2012/04/17	CBC1/2/7/9 CHANGE 0603	
2012/07/12	PLX PCB footprint issue improve	
2013/09/27	Rev 1.1 ATI cross fire logo 改成 "CrossFire" 文字面	
2014/02/13	PCB Rev 1.2 USB 3.0 controller change from VL800 to VL805	Sales request

BLOCK DIAGRAM





CFG 0-17 all internal PULL-UP

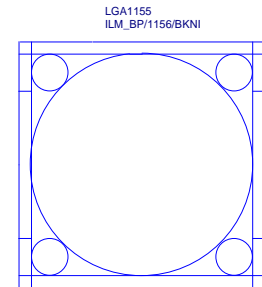


LGA1155A			
M_AAA0	AV27	SA_MA[0]	SA_DQS[0]
M_AAA1	AY24	SA_MA[1]	SA_DQS[0]
M_AAA2	AW24	SA_MA[2]	
M_AAA3	AW23	SA_MA[3]	
M_AAA4	AV23	SA_MA[4]	
M_AAA5	AT24	SA_MA[5]	
M_AAA6	AT23	SA_MA[6]	
M_AAA7	AU22	SA_MA[7]	
M_AAA8	AV22	SA_MA[8]	
M_AAA9	AT22	SA_MA[9]	
M_AAA10	AV28	SA_MA[10]	
M_AAA11	AU21	SA_MA[11]	
M_AAA12	AT21	SA_MA[12]	
M_AAA13	AW32	SA_MA[13]	
M_AAA14	AU20	SA_MA[14]	
M_AAA15	AT20	SA_MA[15]	
(7) M_SWEA	AW29	SA_WE#	
(7) M_SCASA	AV30	SA_CAS#	
(7) M_SRASA	AU28	SA_RAS#	
(7) M_SBAA0	AY29	SA_BS[0]	
(7) M_SBAA1	AW28	SA_BS[1]	
(7) M_SBAA2	AV20	SA_BS[2]	
(7) M-CSA0	AU29	SA_CS#	
(7) M-CSA1	AV32	SA_CS#	
(7) M-CSA2	AW30	SA_CS#	
(7) M-CSA3	AU33	SA_CS#	
(7) M_CKEA0	AV19	SA_CKE[0]	
(7) M_CKEA1	AT19	SA_CKE[1]	
(7) M_CKEA2	AU18	SA_CKE[2]	
(7) M_CKEA3	AV18	SA_CKE[3]	
M_ODT_A0	AV31	SA_ODT[0]	
M_ODT_A1	AU32	SA_ODT[1]	
M_ODT_A2	AU30	SA_ODT[2]	
M_ODT_A3	AW33	SA_ODT[3]	
(7) M_DCLKA0	AY25	SA_CK[0]	
(7) M_DCLKA0	AW25	SA_CK[0]	
(7) M_DCLKA1	AU24	SA_CK[1]	
(7) M_DCLKA1	AU25	SA_CK[1]	
(7) M_DCLKA2	AW27	SA_CK[2]	
(7) M_DCLKA2	AY27	SA_CK[2]	
(7) M_DCLKA3	AU26	SA_CK[3]	
(7) M_DCLKA3	AW26	SA_CK[3]	
(7,8) M_DDR3_RST	MR1	SM_DRAMRST#	
	MBC8	0.1u4/X7R/16V/K/X	
AV13	SA_DQS[8]		
AV12	SA_DQS[8]		
AU12	SA_ECC_CB[0]		
AU14	SA_ECC_CB[1]		
AW13	SA_ECC_CB[2]		
AY13	SA_ECC_CB[3]		
AU13	SA_ECC_CB[4]		
AY12	SA_ECC_CB[5]		
AW12	SA_ECC_CB[6]		
AW12	SA_ECC_CB[7]		
DDR_0			
1 OF 10			
LGA1155[10SC1-F01155-01R]			

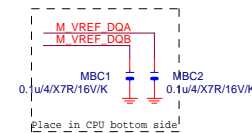
www.aitech1.ru

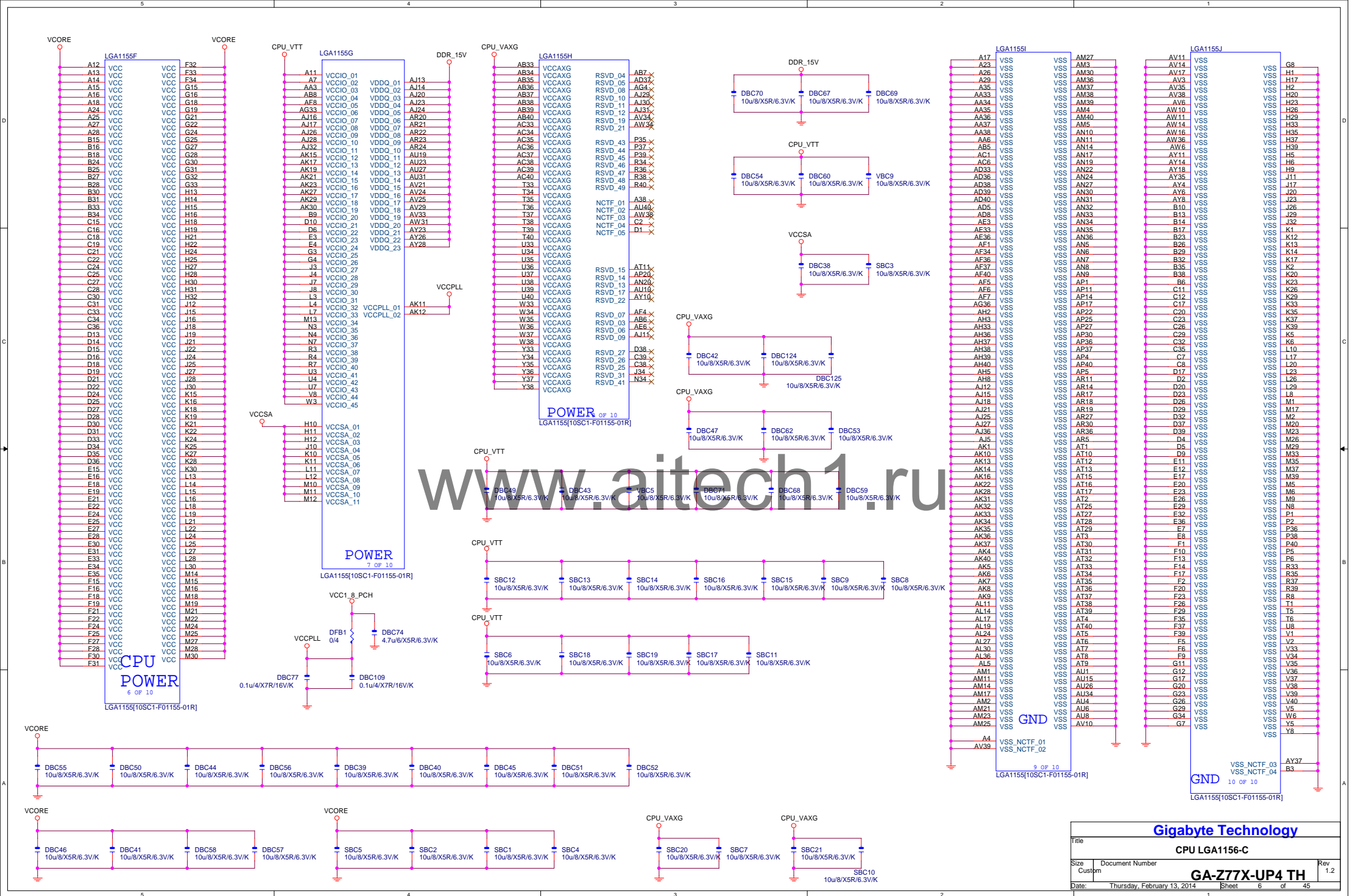
(7) M_ODT_A[0..3]	M_ODT_A[0..3]
(8) M_ODT_B[0..3]	M_ODT_B[0..3]
(7) M_DA[0..63]	M_DA[0..63]
(8) M_DB[0..63]	M_DB[0..63]
(7) M_DQSA[0..7]	M_DQSA[0..7]
(7) M_-DQSA[0..7]	M_-DQSA[0..7]
(7) M_AA[0..15]	M_AA[0..15]
(8) M_AAB[0..15]	M_AAB[0..15]
(8) M_DQSB[0..7]	M_DQSB[0..7]
(8) M_-DQSB[0..7]	M_-DQSB[0..7]

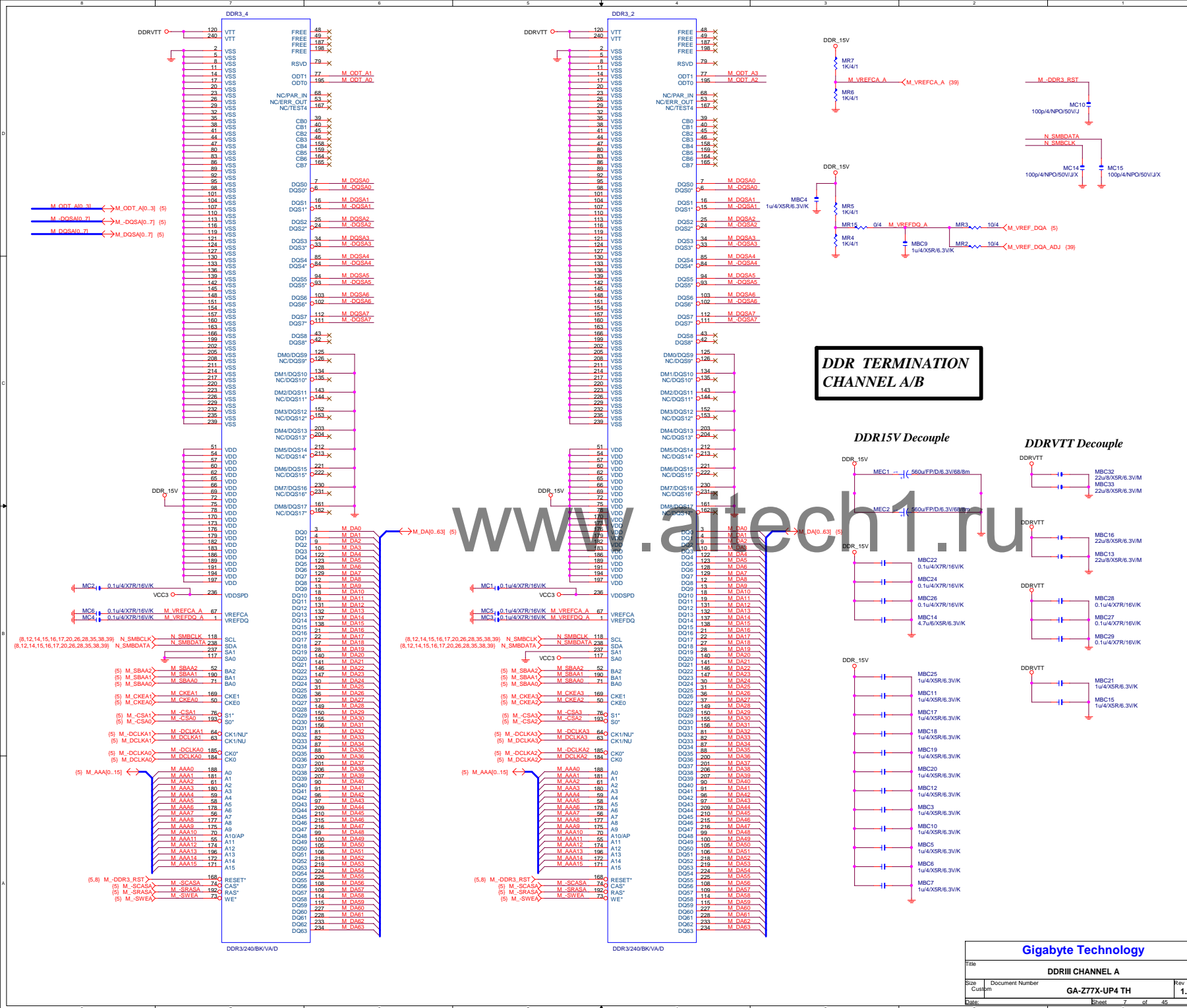
LGA1155B			
M_AAB0	AK24	SB_MA[0]	SB_DQS[0]
M_AAB1	AM20	SB_MA[1]	SB_DQS[0]
M_AAB2	AM19	SB_MA[2]	
M_AAB3	AK18	SB_MA[3]	
M_AAB4	AP19	SB_MA[4]	
M_AAB5	AP18	SB_MA[5]	
M_AAB6	AM18	SB_MA[6]	
M_AAB7	AL18	SB_MA[7]	
M_AAB8	AY17	SB_MA[8]	
M_AAB9	AY17	SB_MA[9]	
M_AAB10	AN23	SB_MA[10]	
M_AAB11	AU17	SB_MA[11]	
M_AAB12	AT18	SB_MA[12]	
M_AAB13	AR26	SB_MA[13]	
M_AAB14	AY16	SB_MA[14]	
M_AAB15	AV16	SB_MA[15]	
(8) M_SWEB	AR25	SB_WE#	
(8) M_SCASB	AK25	SB_CAS#	
(8) M_SRASB	AP24	SB_RAS#	
(8) M_SBAB0	AP23	SB_BS[0]	
(8) M_SBAB1	AM24	SB_BS[1]	
(8) M_SBAB2	AW17	SB_BS[2]	
(8) M-CSB0	AN25	SB_CS#	
(8) M-CSB1	AN26	SB_CS#	
(8) M-CSB2	AL26	SB_CS#	
(8) M-CSB3	AT26	SB_CS#	
(8) M_CKEB0	AU16	SB_CKE[0]	
(8) M_CKEB1	AY15	SB_CKE[1]	
(8) M_CKEB2	AW15	SB_CKE[2]	
(8) M_CKEB3	AV15	SB_CKE[3]	
M_ODT_B0	AL26	SB_ODT[0]	
M_ODT_B1	AP26	SB_ODT[1]	
M_ODT_B2	AM26	SB_ODT[2]	
M_ODT_B3	AK26	SB_ODT[3]	
(8) M_DCLKB0	AL21	SB_CK[0]	
(8) M_DCLKB0	AL22	SB_CK[0]	
(8) M_DCLKB1	AL20	SB_CK[1]	
(8) M_DCLKB1	AK20	SB_CK[1]	
(8) M_DCLKB2	AL23	SB_CK[2]	
(8) M_DCLKB2	AM22	SB_CK[2]	
(8) M_DCLKB3	AP21	SB_CK[3]	
(8) M_DCLKB3	AN21	SB_CK[3]	
(8) M_VREF_DQB	AH1	FC_AH1	
(7) M_VREF_DQB	AH4	FC_AH4	
AN16	SB_DQS[8]		
AN15	SB_DQS[8]		
AL16	SB_ECC_CB[0]		
AM16	SB_ECC_CB[1]		
AP16	SB_ECC_CB[2]		
AL15	SB_ECC_CB[3]		
AM15	SB_ECC_CB[4]		
AP15	SB_ECC_CB[5]		
AP15	SB_ECC_CB[7]		
SB_DQS[4]	AN29	M_DQSB4	
SB_DQS[4]	AN28	M_-DQSB4	
SB_DQS[32]	AR28	M_DB32	
SB_DQS[33]	AP23	M_DB33	
SB_DQS[34]	AL28	M_DB34	
SB_DQS[35]	AL29	M_DB35	
SB_DQS[36]	AP28	M_DB36	
SB_DQS[37]	AP29	M_DB37	
SB_DQS[38]	AM28	M_DB38	
SB_DQS[39]	AM29	M_DB39	
SB_DQS[5]	AP33	M_DQSB5	
SB_DQS[5]	AR33	M_-DQSB5	
SB_DQ[40]	AP32	M_DB40	
SB_DQ[41]	AP31	M_DB41	
SB_DQ[42]	AP35	M_DB42	
SB_DQ[43]	AP34	M_DB43	
SB_DQ[44]	AR32	M_DB44	
SB_DQ[45]	AR31	M_DB45	
SB_DQ[46]	AR35	M_DB46	
SB_DQ[47]	AR34	M_DB47	
SB_DQS[6]	AL33	M_DQSB6	
SB_DQS[6]	AM33	M_-DQSB6	
SB_DQ[48]	AM32	M_DB48	
SB_DQ[49]	AM31	M_DB49	
SB_DQ[50]	AL35	M_DB50	
SB_DQ[51]	AL32	M_DB51	
SB_DQ[52]	AM34	M_DB52	
SB_DQ[53]	AL31	M_DB53	
SB_DQ[54]	AM35	M_DB54	
SB_DQ[55]	AL34	M_DB55	
SB_DQS[7]	AG35	M_DQSB7	
SB_DQS[7]	AG34	M_-DQSB7	
SB_DQ[56]	AH35	M_DB56	
SB_DQ[57]	AH34	M_DB57	
SB_DQ[58]	AE34	M_DB58	
SB_DQ[59]	AE35	M_DB59	
SB_DQ[60]	AJ35	M_DB60	
SB_DQ[61]	AJ34	M_DB61	
SB_DQ[62]	AF33	M_DB62	
SB_DQ[63]	AF35	M_DB63	
DDR_1			
2 OF 10			
LGA1155[10SC1-F01155-01R]			

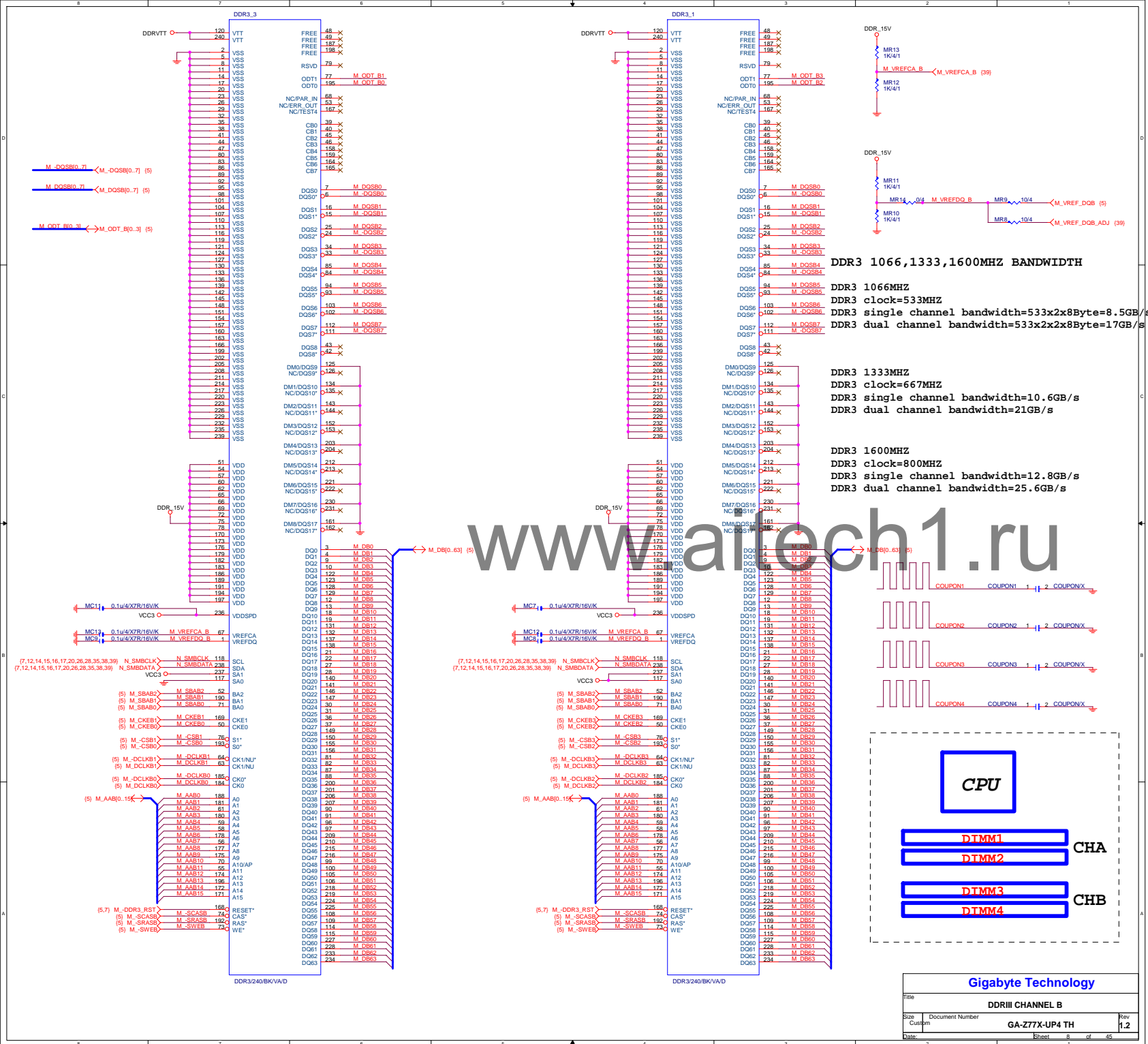


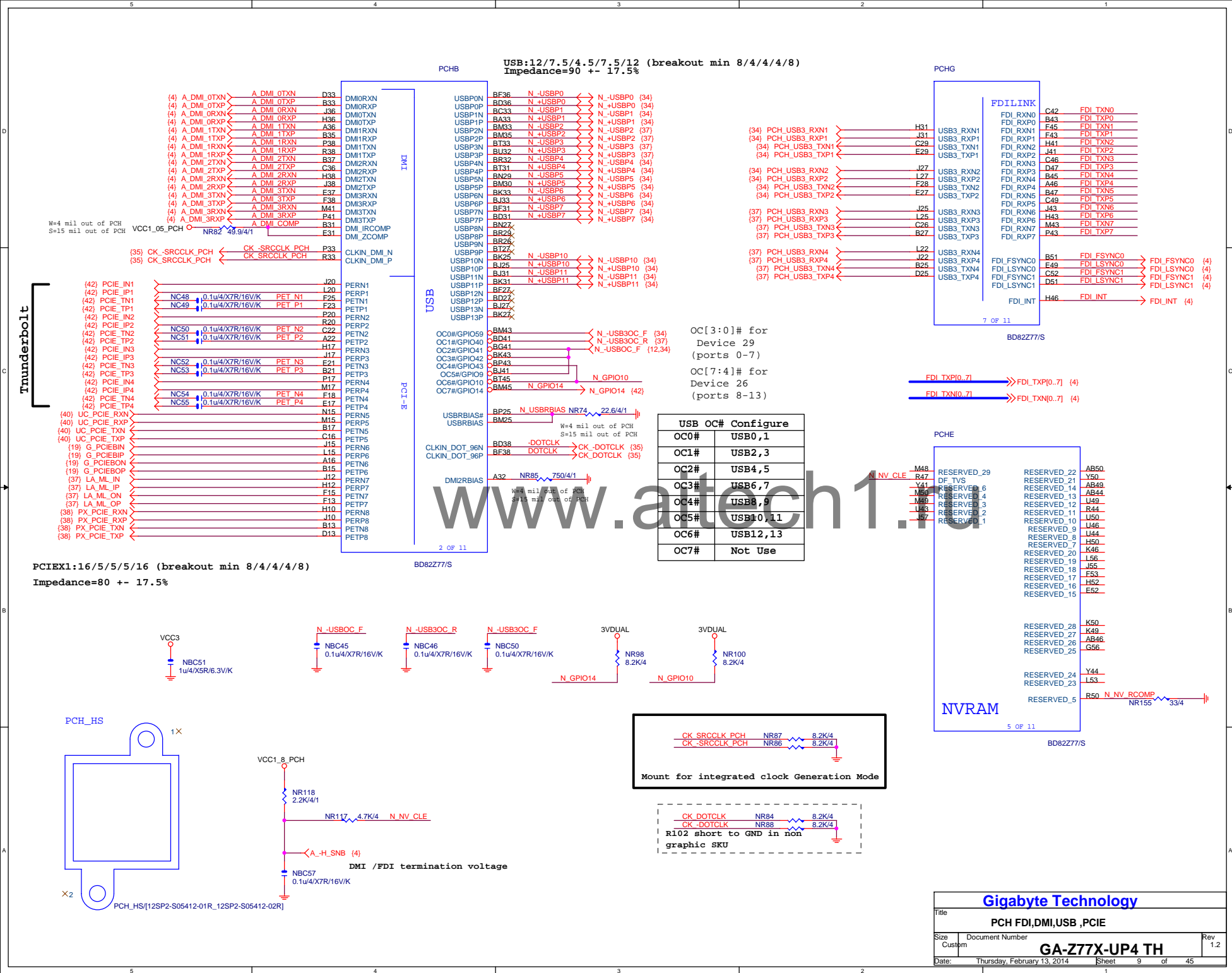
Need check the new CPU ME

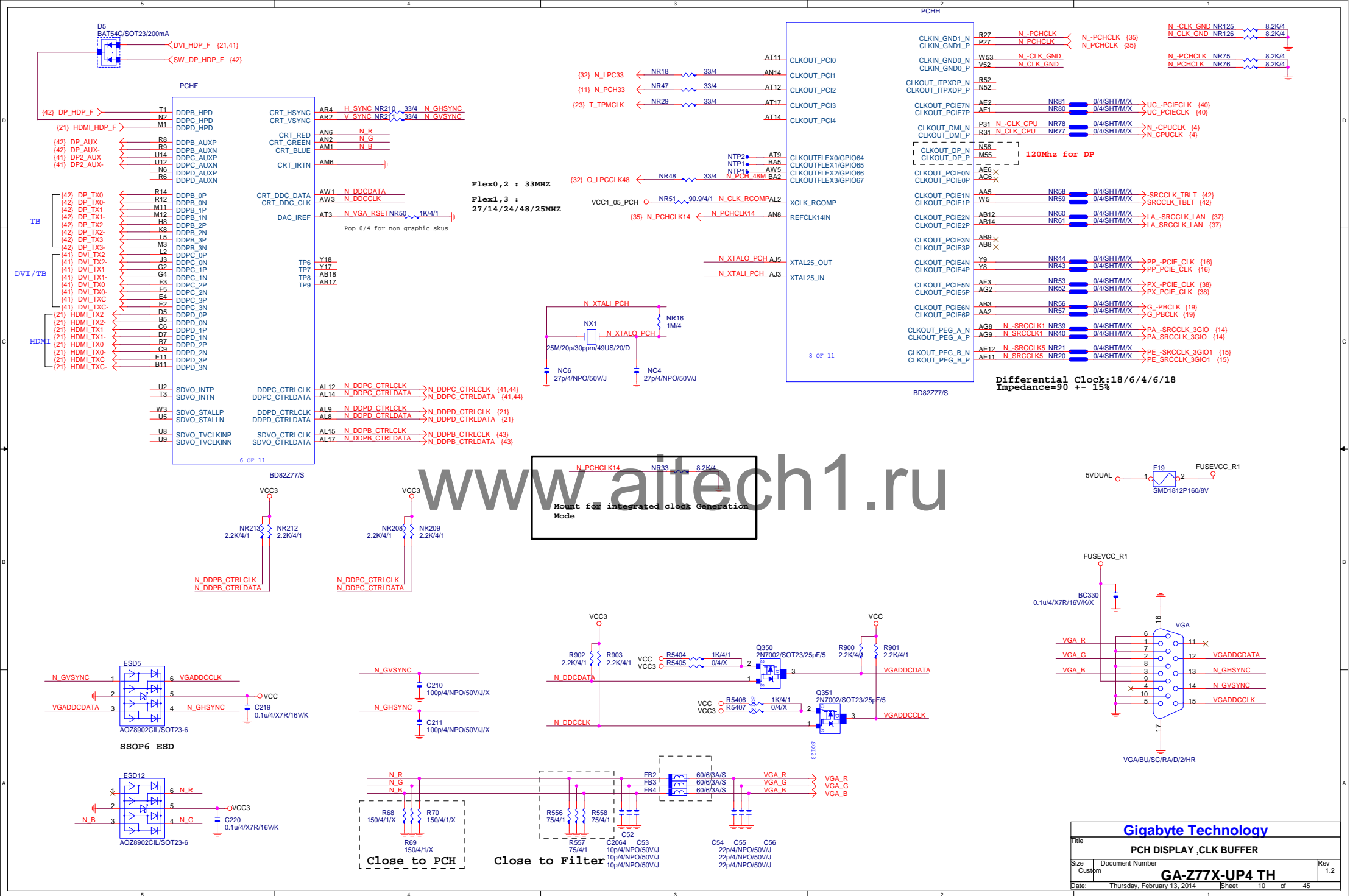




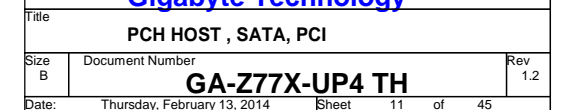


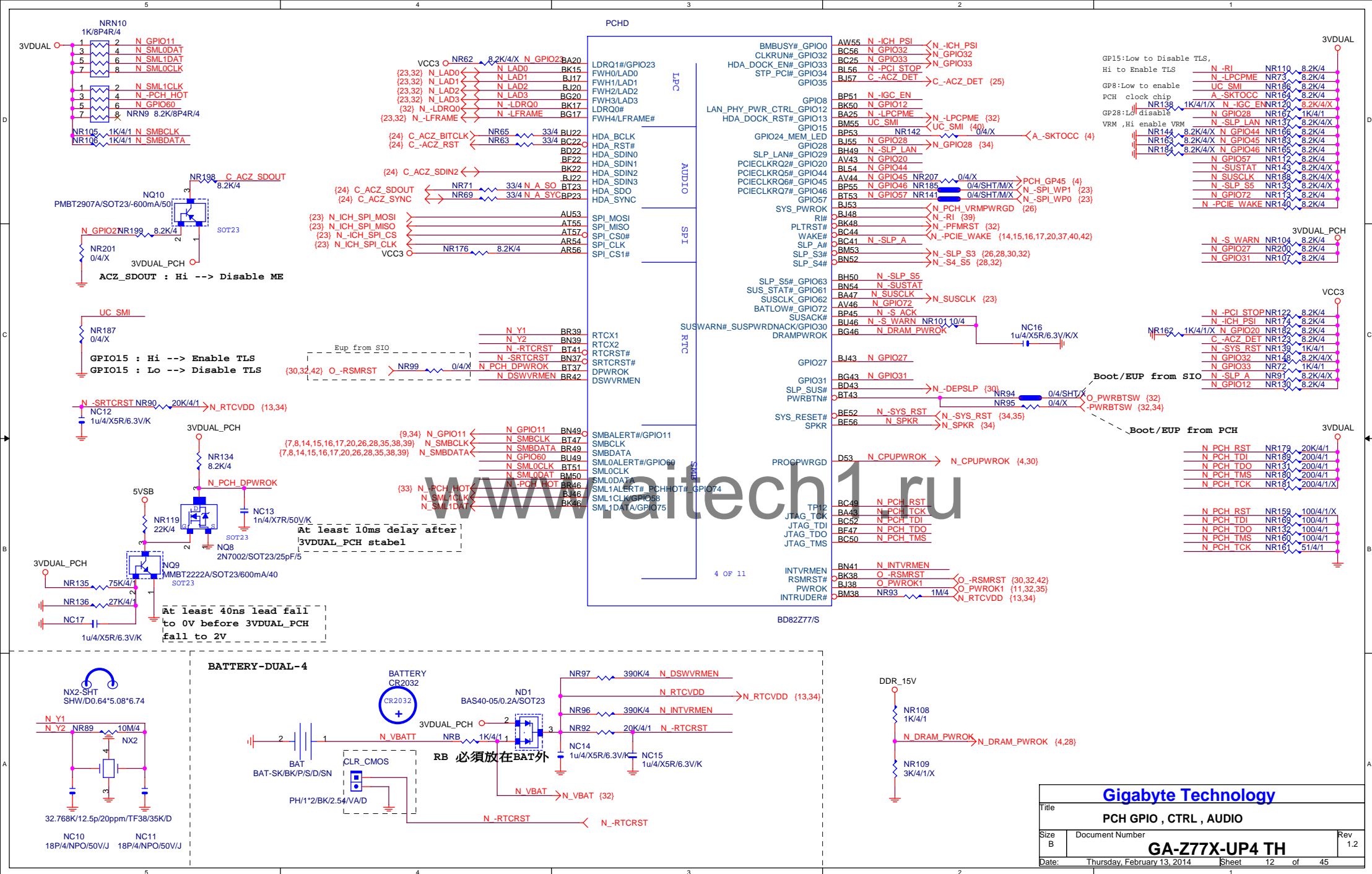


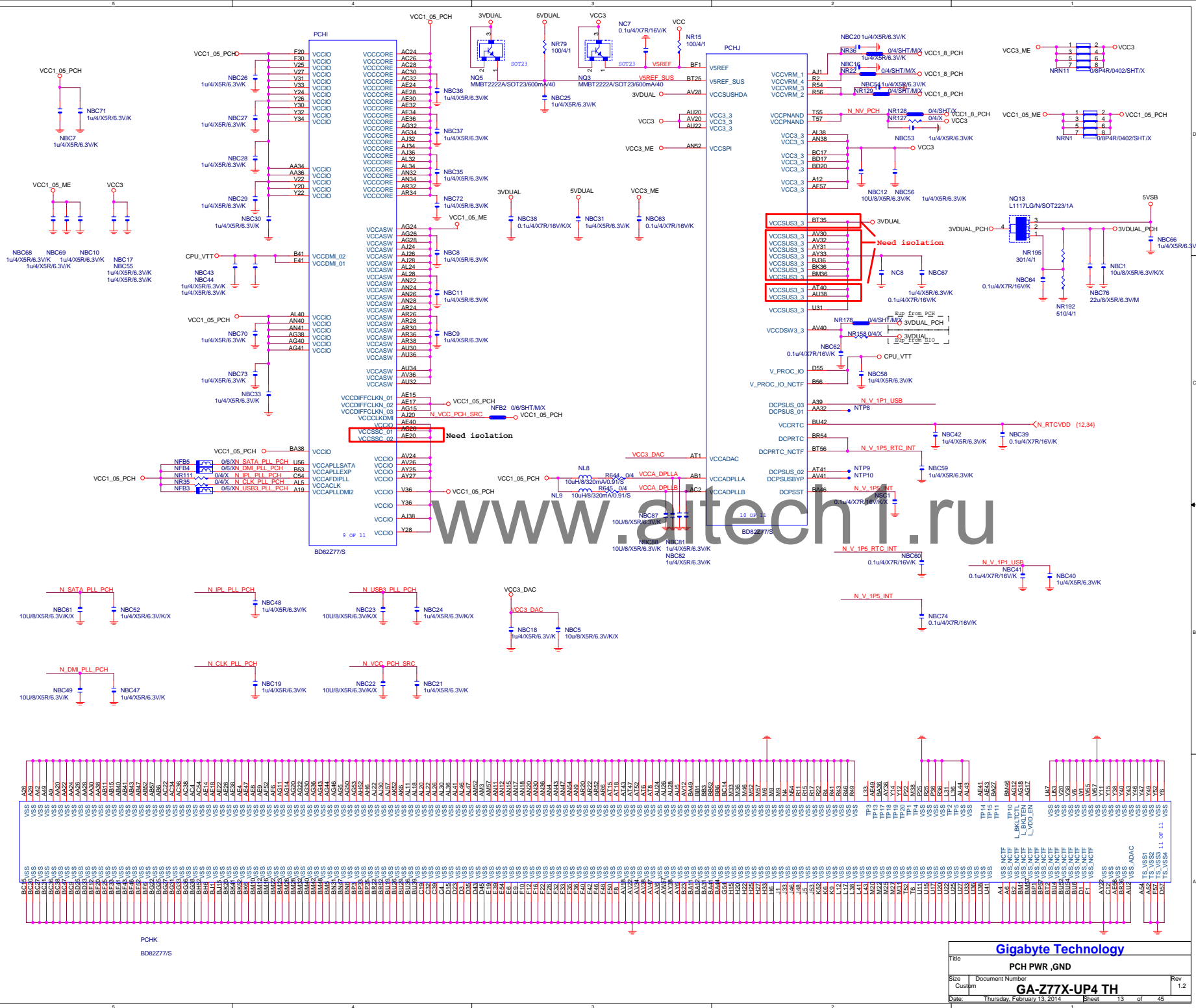


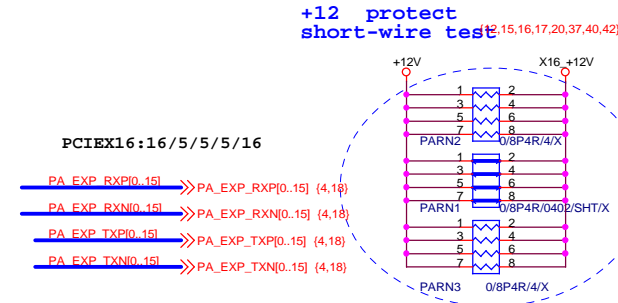
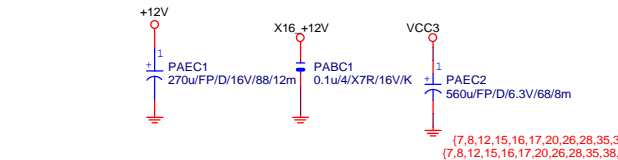


PCHC









PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP SW TXN15 C

PA EXP SW RXP8.15	>>>PA_EXP_SW_RXP[8..15]	(18)
PA EXP SW RXN8.15	>>>PA_EXP_SW_RXN[8..15]	(18)
PA EXP SW TXP8.15	>>>PA_EXP_SW_TXP[8..15]	(18)
PA EXP SW TXN8.15	>>>PA_EXP_SW_TXN[8..15]	(18)

PCI-E REV:1.1--> 2.5GHZ

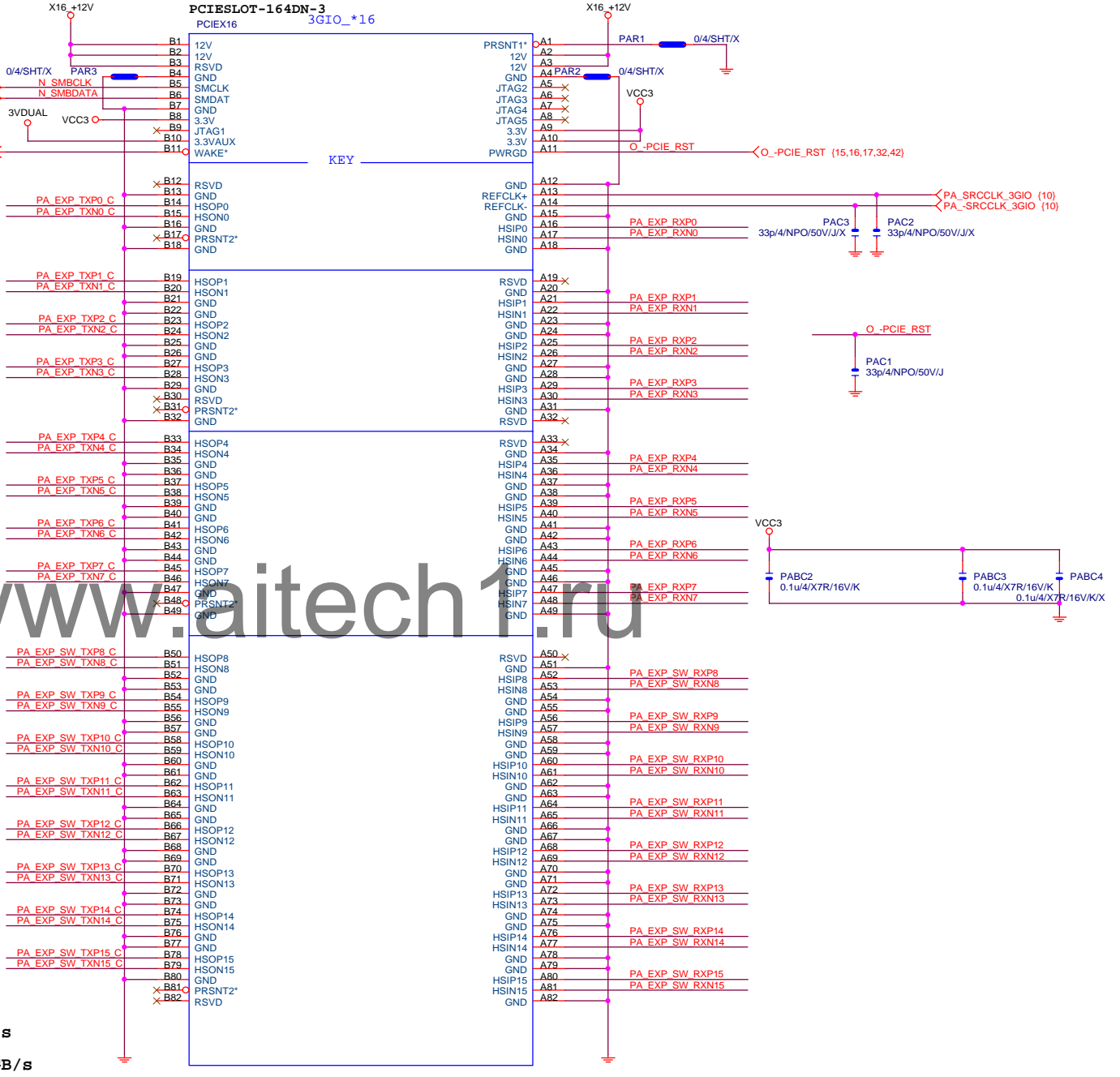
PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

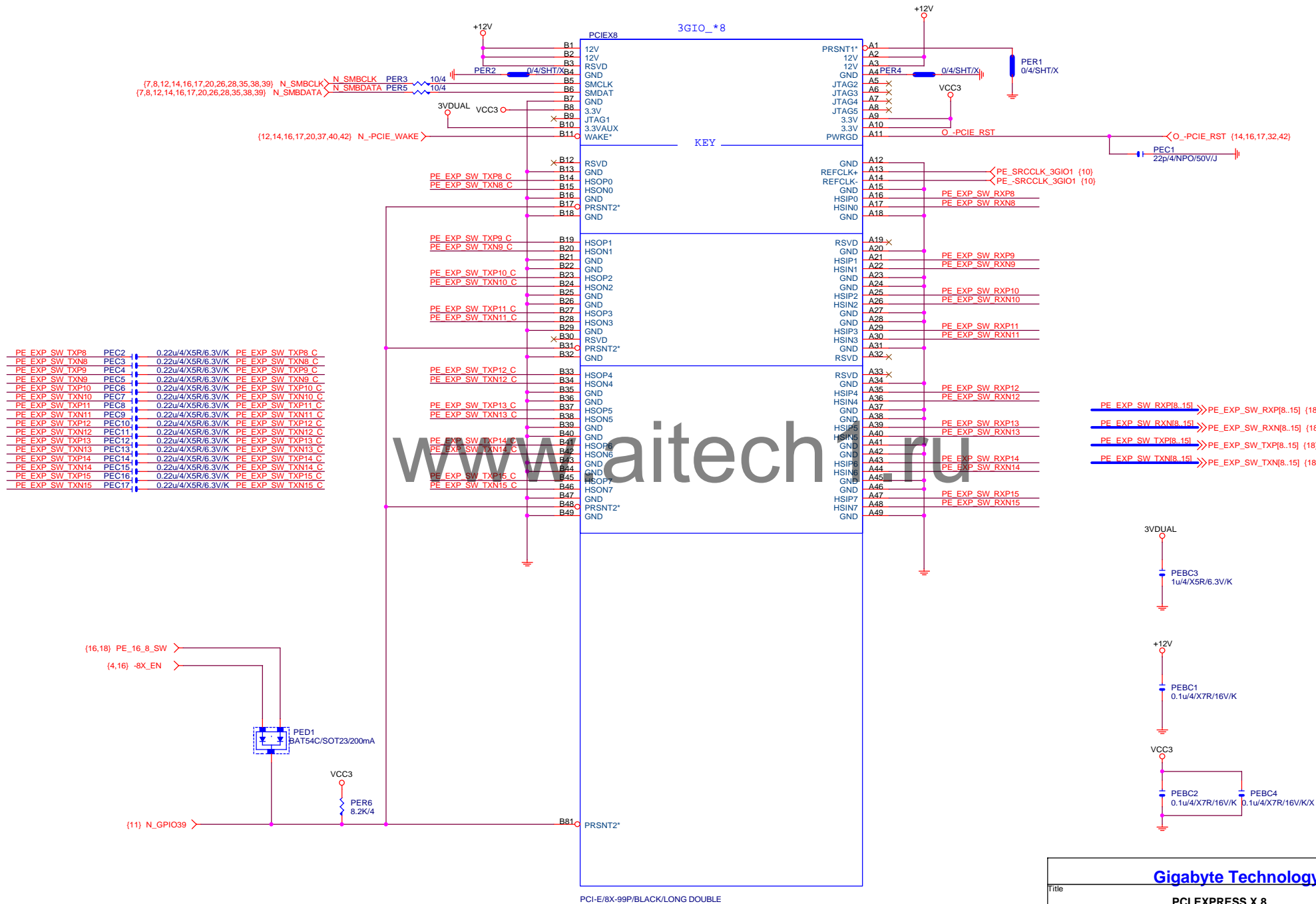
PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

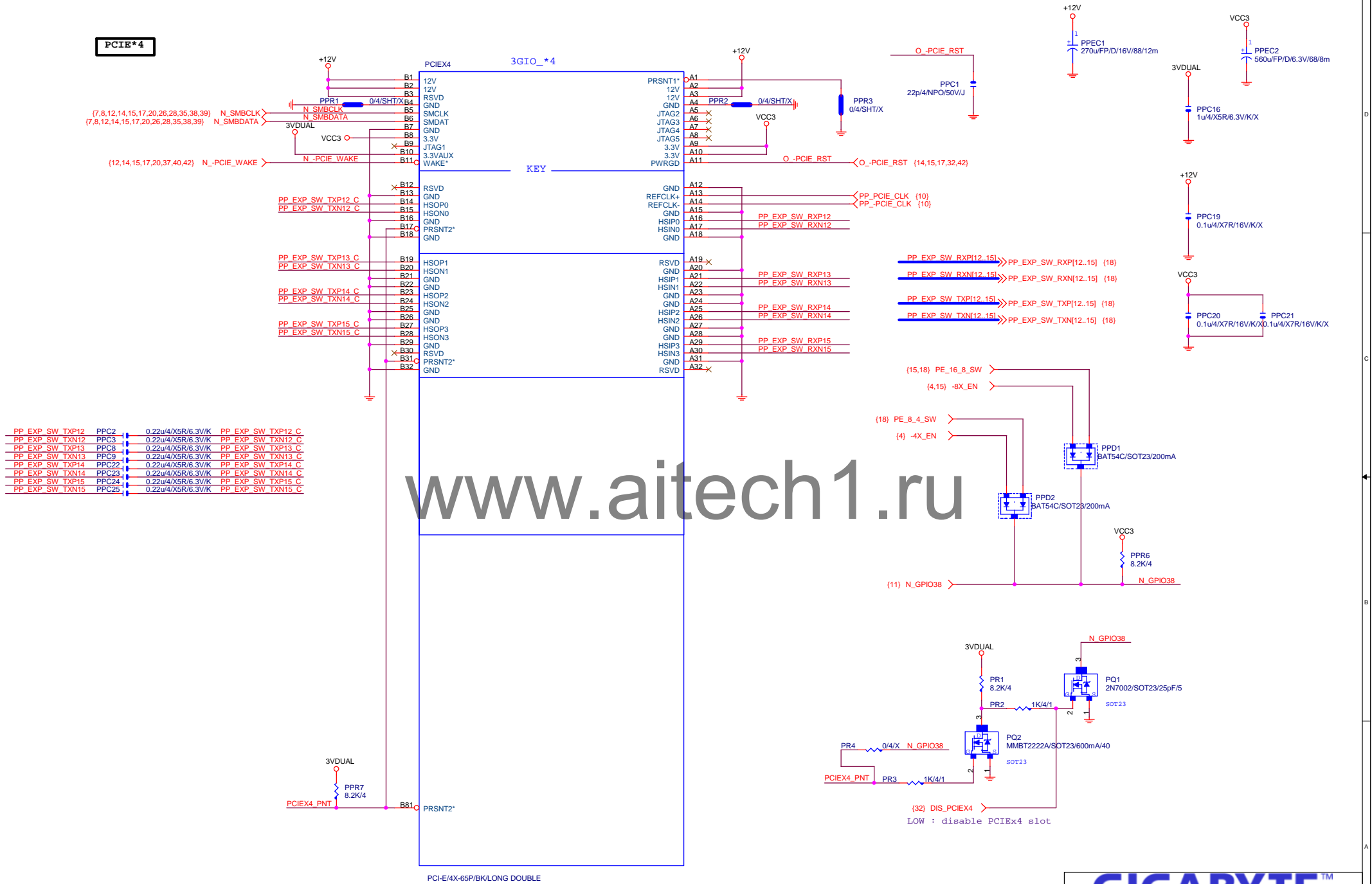
PCI-E REV:2.0--> 5GHZ

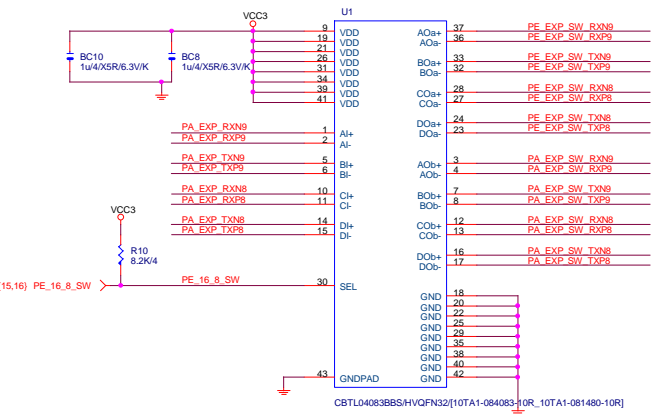


Gigabyte Technology			
Title			
PCI EXPRESS X 16			
Size	Document Number	GA-Z77X-UP4 TH	
Custom			Rev 1.2
Date:	Thursday, February 13, 2014	Sheet	14 of 45

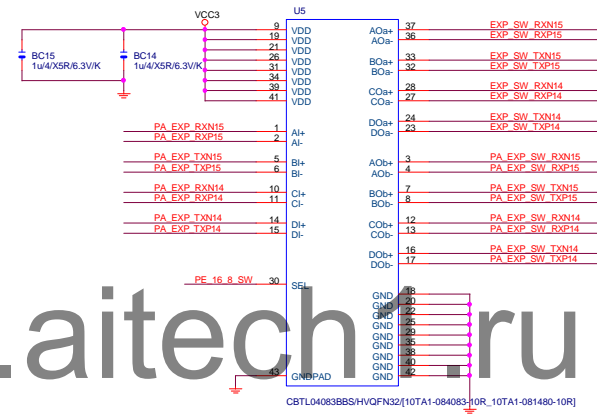
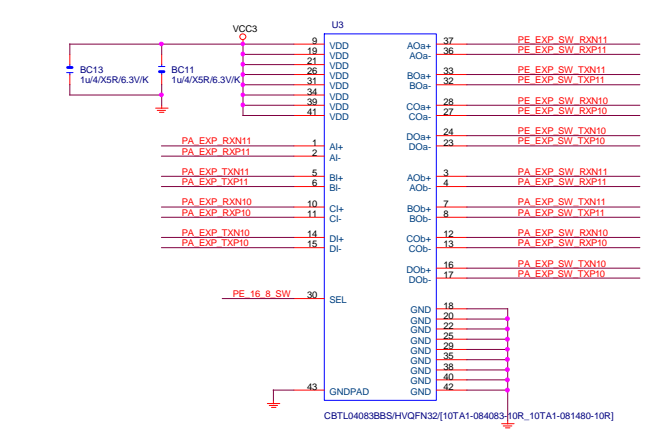
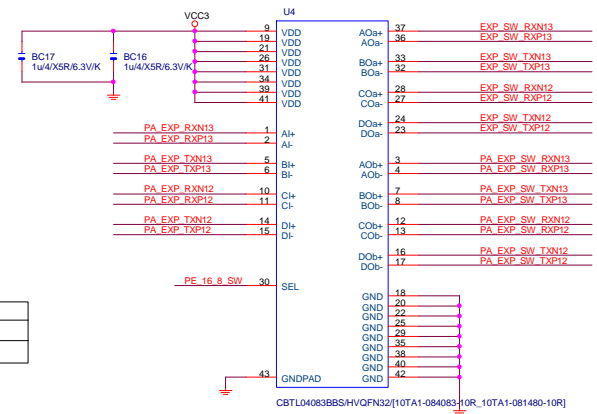


PCIE*4

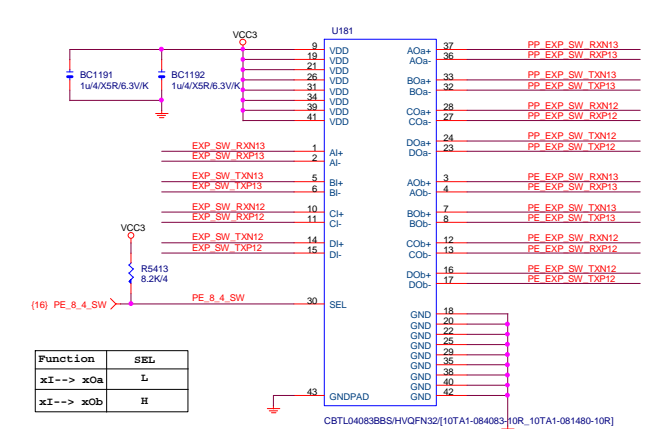




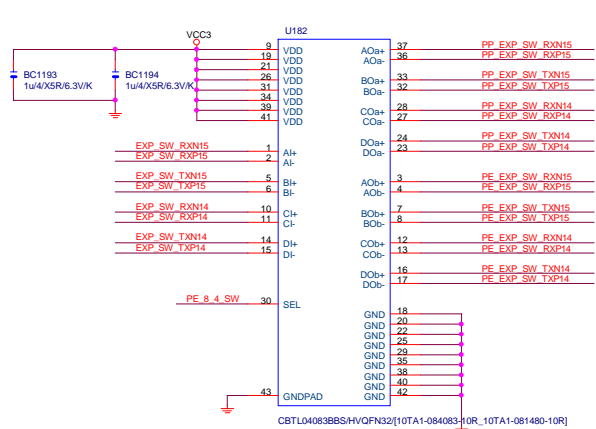
Function	SEL
xI--> xOa	L
xI--> xOb	H

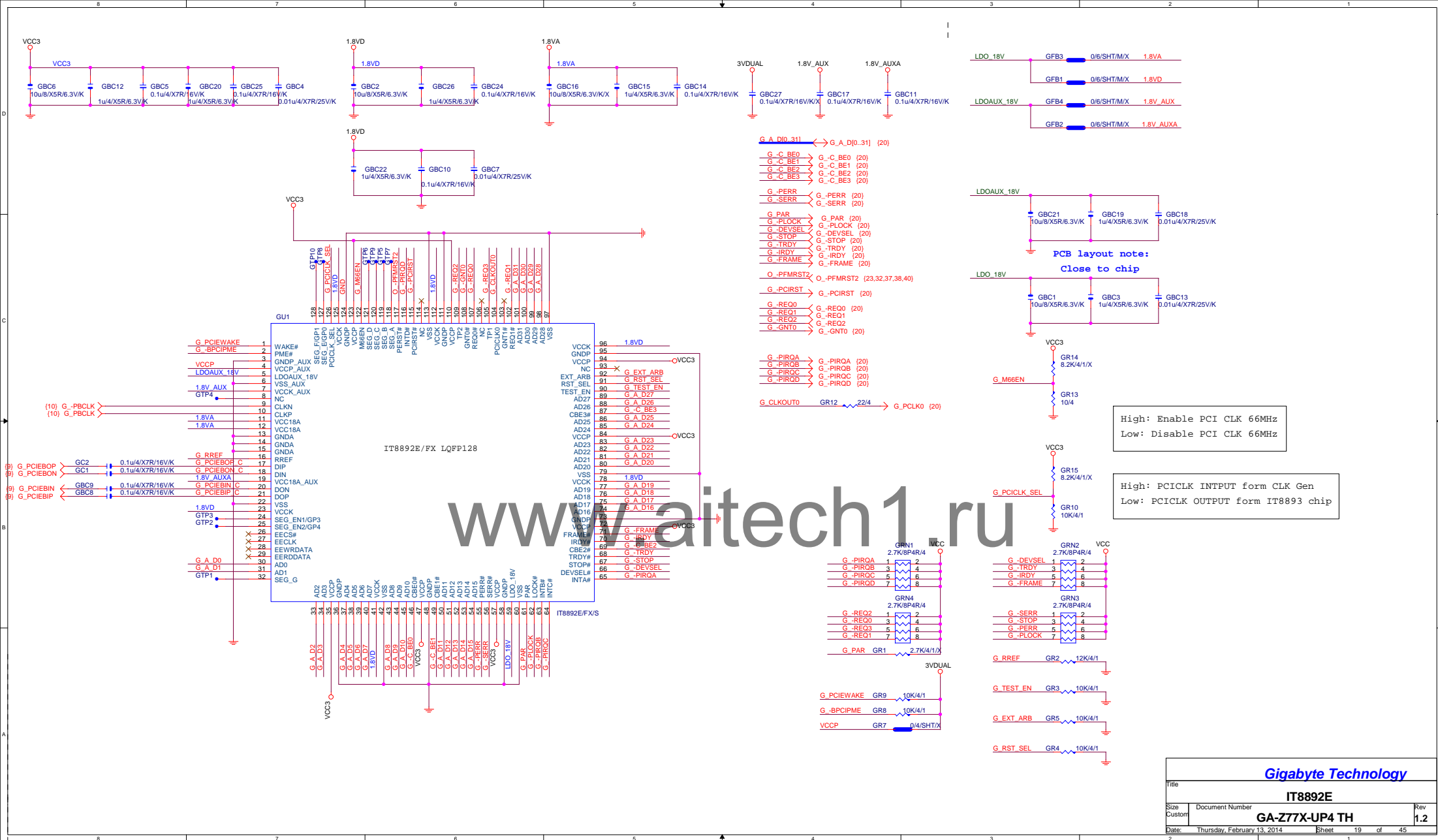


- PA EXP RXN0.15] >> PA_EXP_RXN0.15] (4,14)
- PA EXP RXN0.15] >> PA_EXP_RXN0.15] (4,14)
- PA EXP TXN0.15] >> PA_EXP_TXN0.15] (4,14)
- PA EXP TXN0.15] >> PA_EXP_TXN0.15] (4,14)
- PA EXP SW RXN8.15] >> PA_EXP_SW_RXN8.15] (14)
- PA EXP SW RXN8.15] >> PA_EXP_SW_RXN8.15] (14)
- PA EXP SW TXN8.15] >> PA_EXP_SW_TXN8.15] (14)
- PA EXP SW TXN8.15] >> PA_EXP_SW_TXN8.15] (14)
- PE EXP SW RXN8.15] >> PE_EXP_SW_RXN8.15] (15)
- PE EXP SW RXN8.15] >> PE_EXP_SW_RXN8.15] (15)
- PE EXP SW TXN8.15] >> PE_EXP_SW_TXN8.15] (15)
- PE EXP SW TXN8.15] >> PE_EXP_SW_TXN8.15] (15)
- PP EXP SW RXN12.15] >> PP_EXP_SW_RXN12.15] (16)
- PP EXP SW RXN12.15] >> PP_EXP_SW_RXN12.15] (16)
- PP EXP SW TXN12.15] >> PP_EXP_SW_TXN12.15] (16)
- PP EXP SW TXN12.15] >> PP_EXP_SW_TXN12.15] (16)

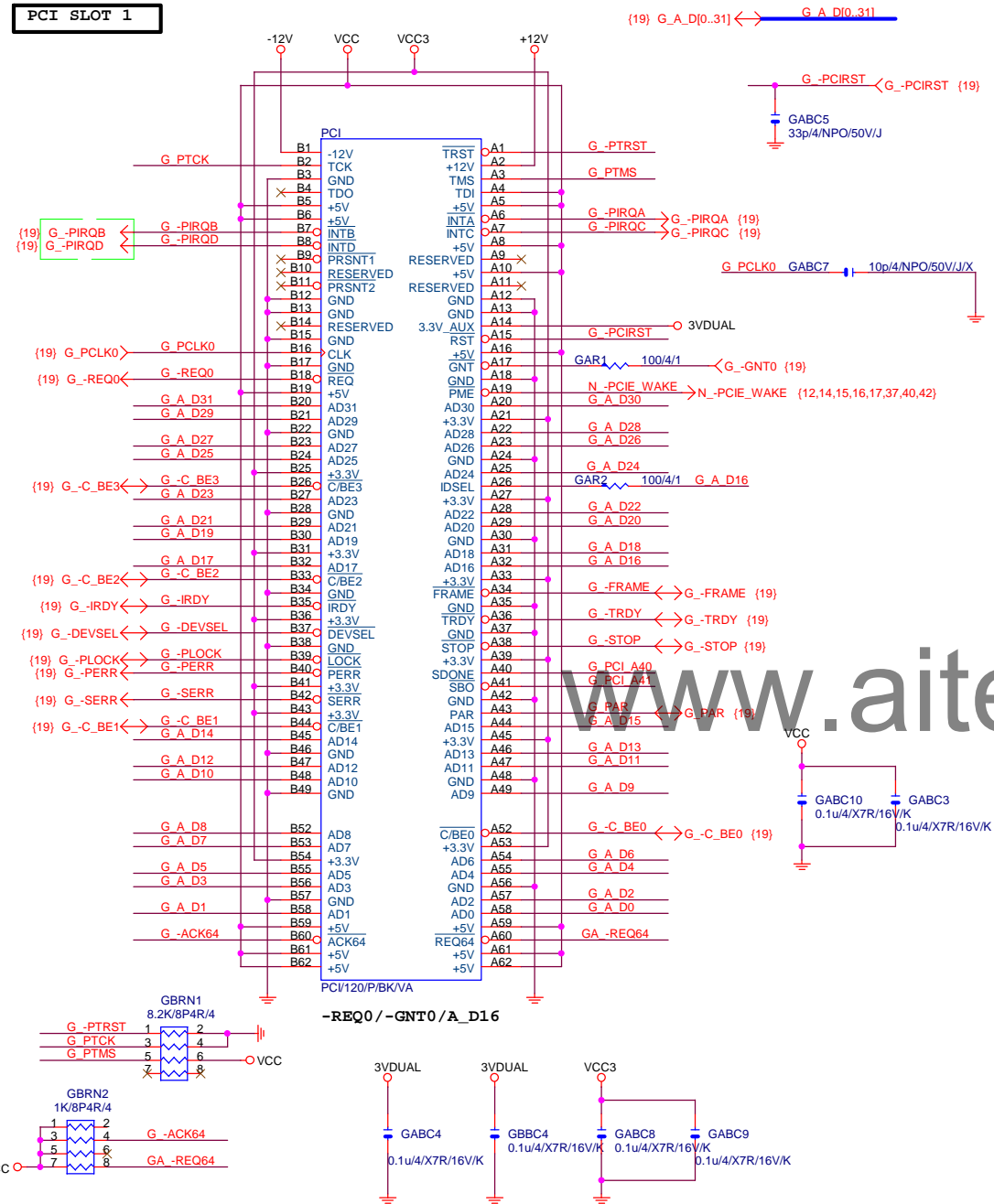


Function	SEL
xI--> xOa	L
xI--> xOb	H

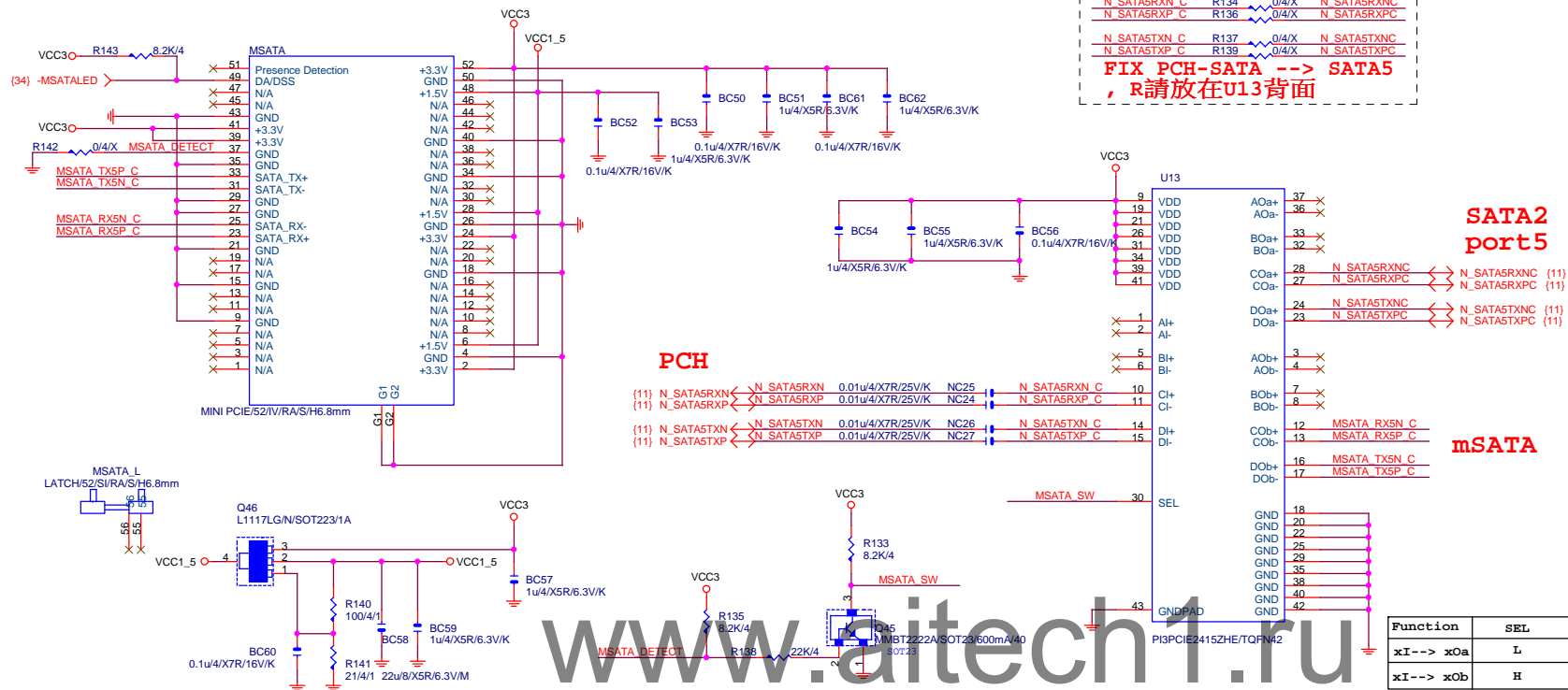




PCI SLOT 1



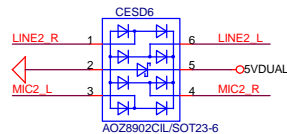
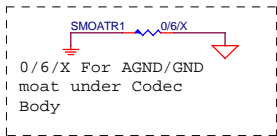
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PCI SLOT 1			
Size	Document Number		Rev
Custom	GA-Z77X-UP4 TH		1.2
Date:	Thursday, February 13, 2014		Sheet 20 of 45

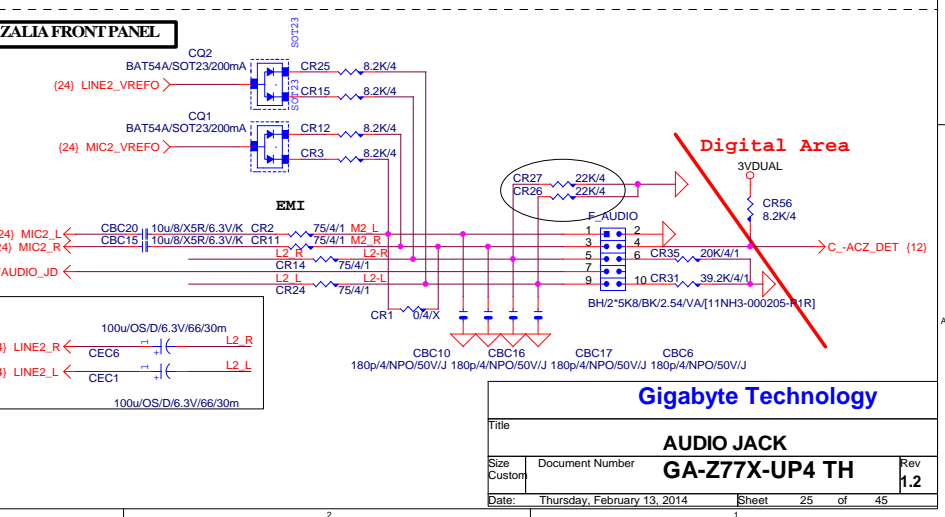
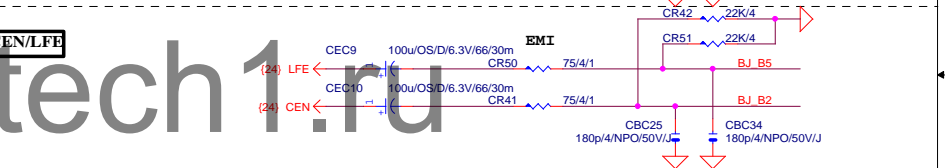
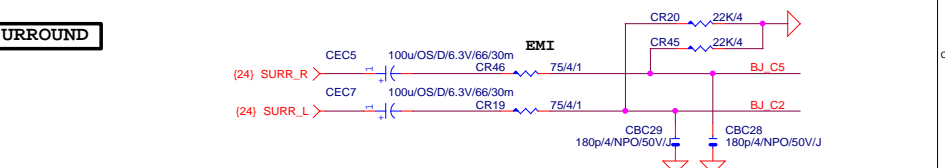
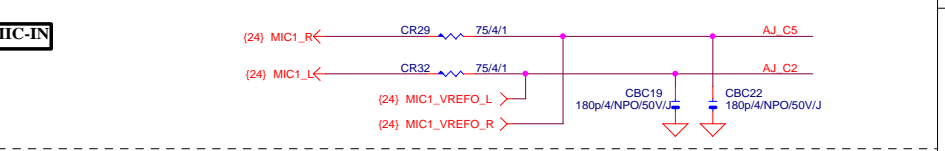
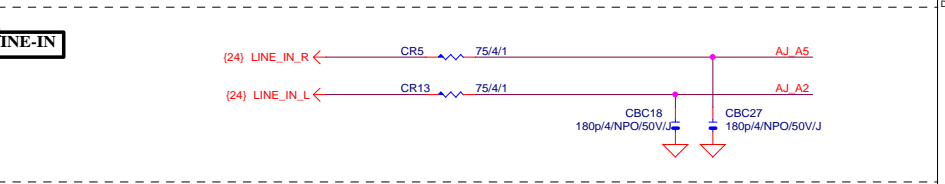
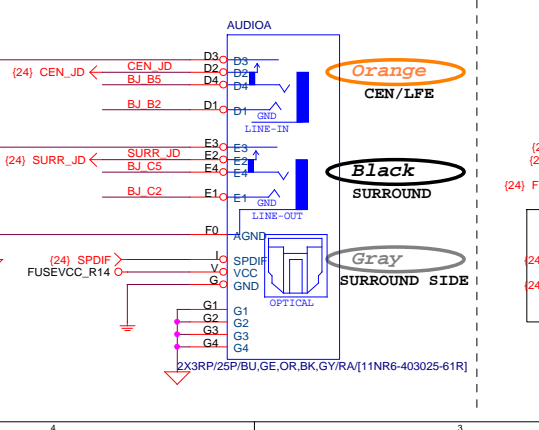
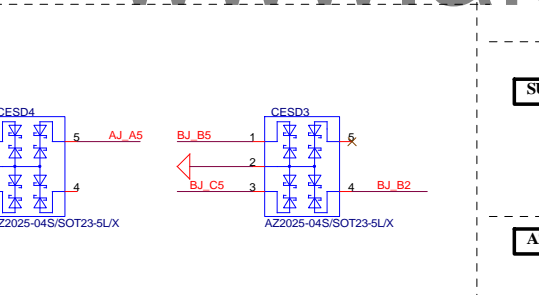
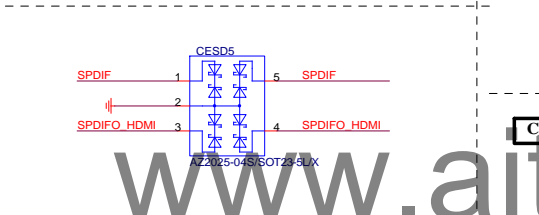
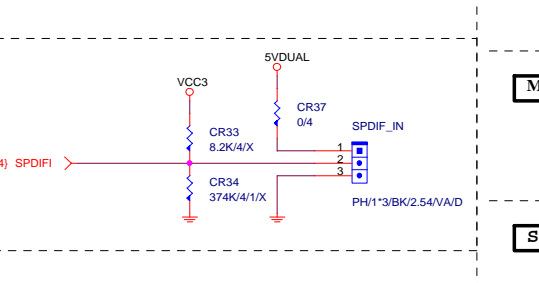
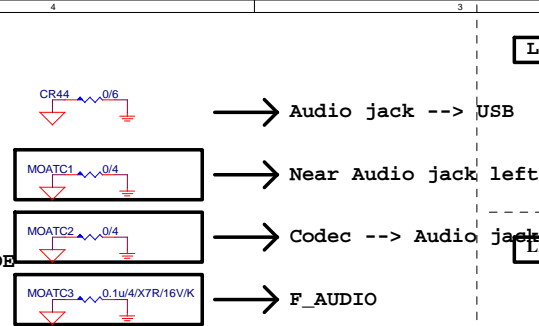


GIGABYTE™

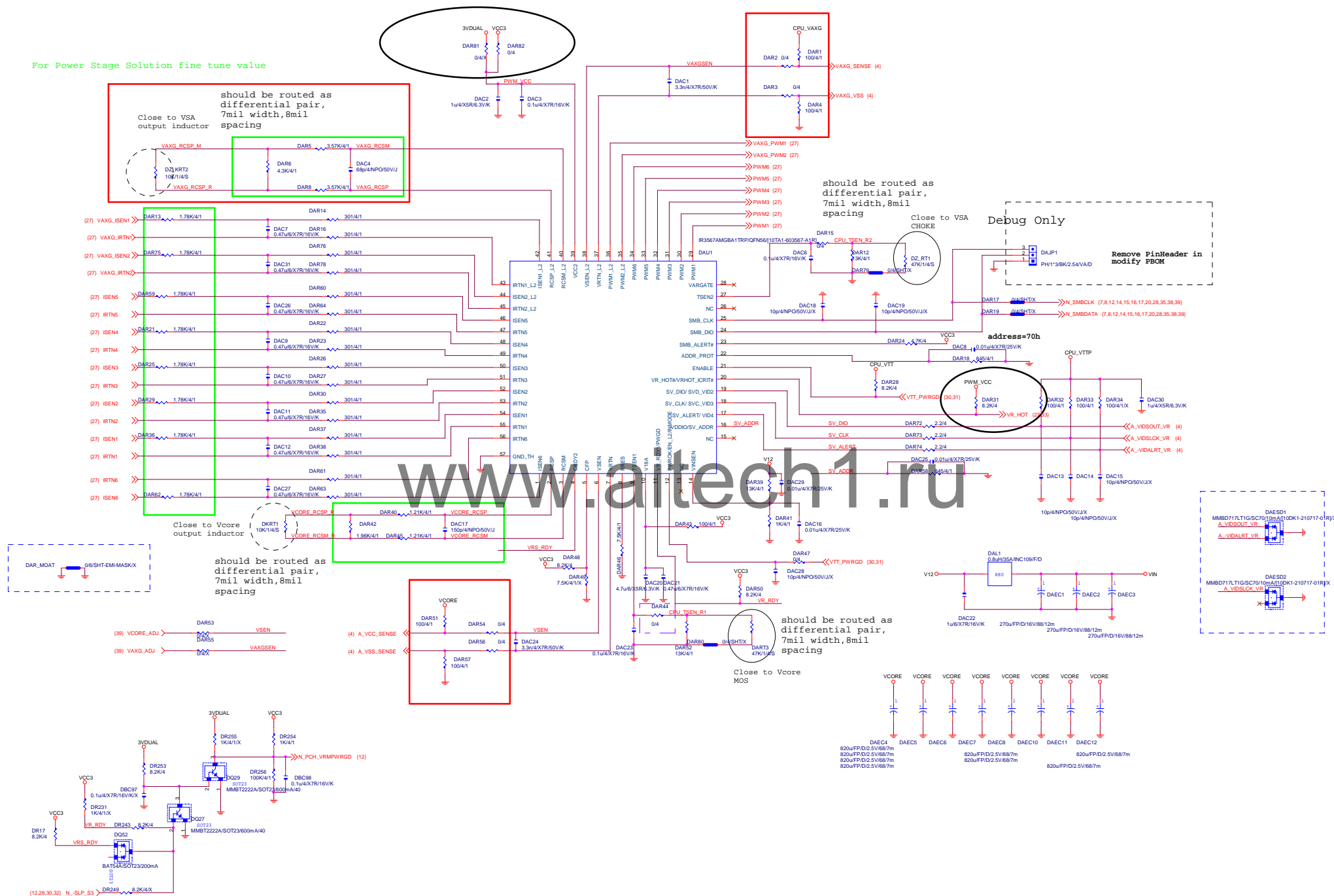
Title		
mSATA Conn		
Size	Document Number	Rev
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CR7/CR9/CR5/CR13/
CR29/CR32/CR46/CR19/
CR50/CR41/CR21/CR47/
CR2/CR11/CR14/CR24





For Power Stage Solution fine tune value



(3553 / 3550 co-lay)



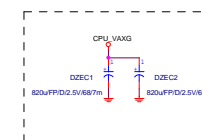
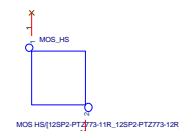
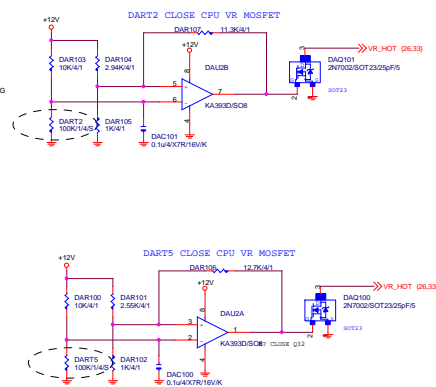
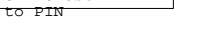
VCORE-PHASE5

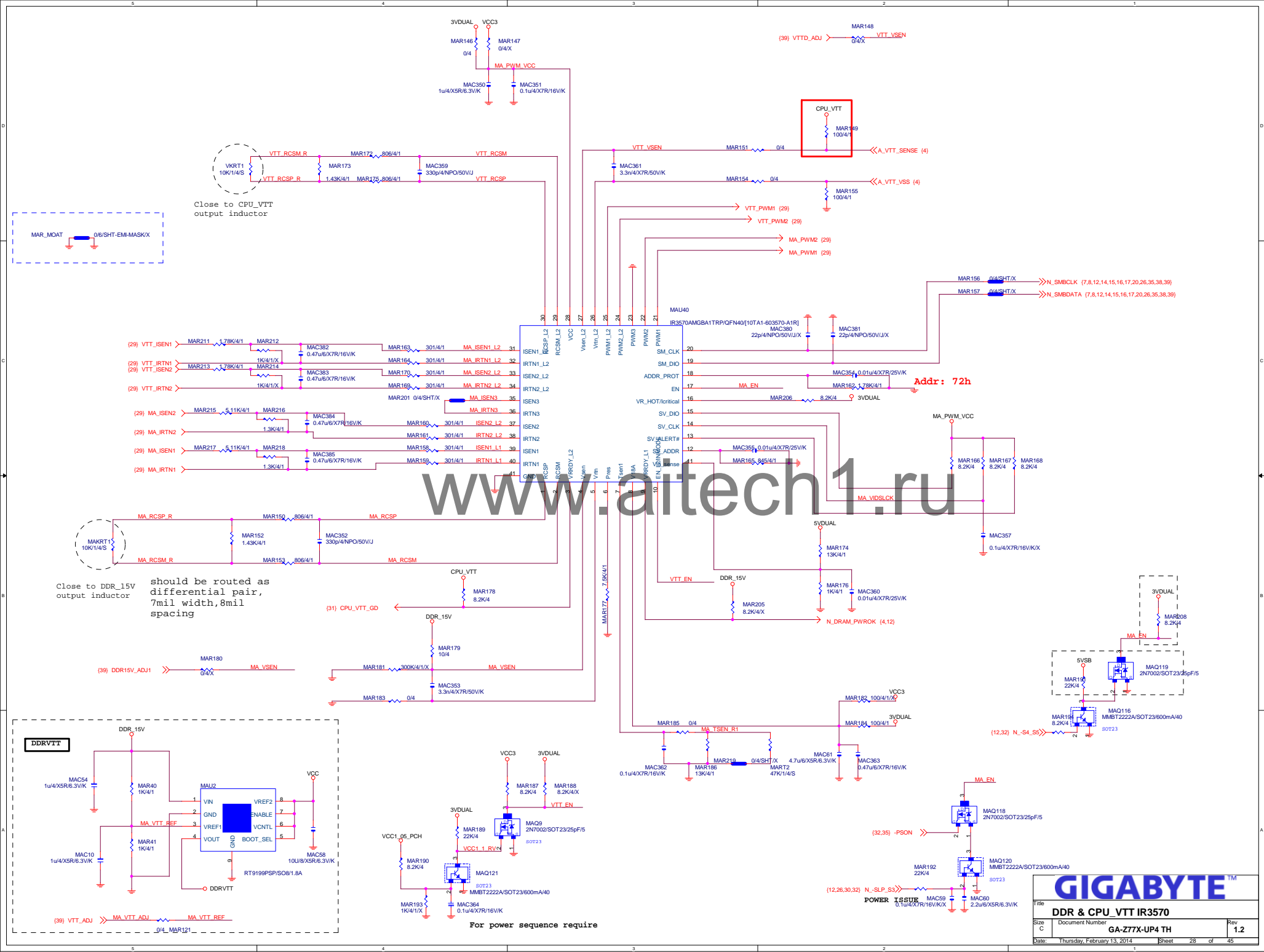


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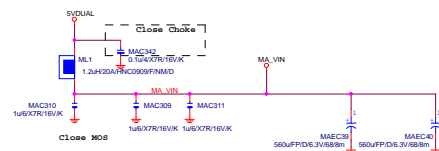
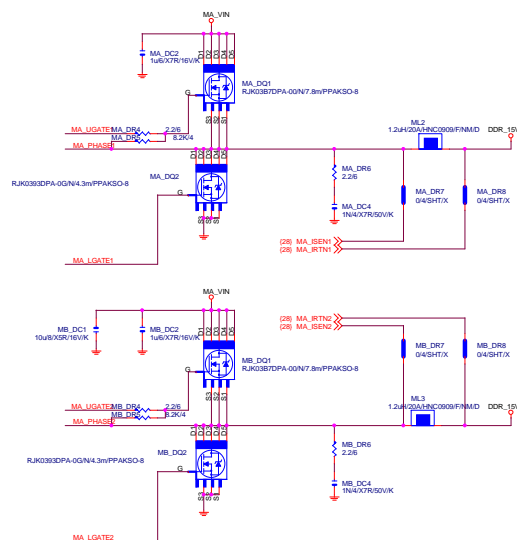
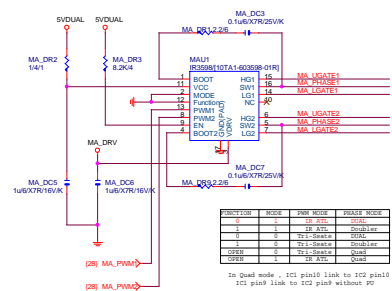


VAXG Phase



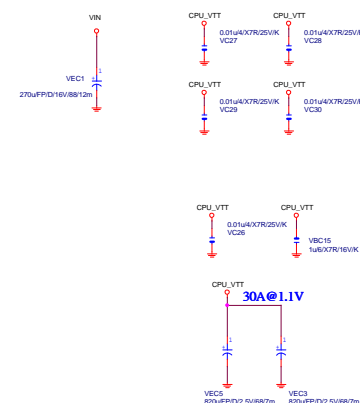
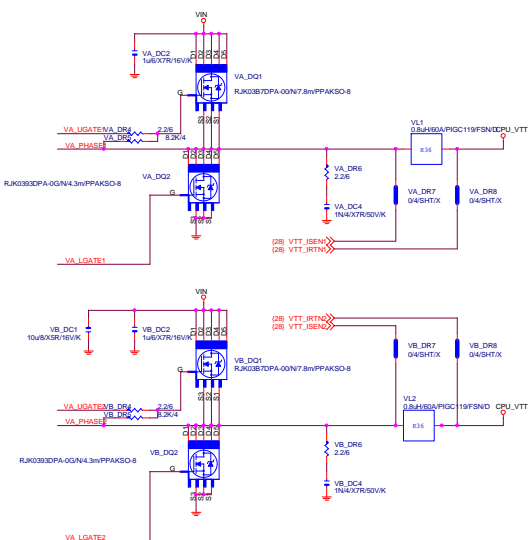
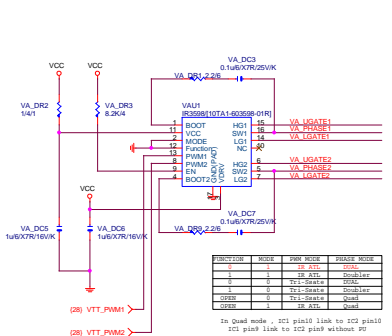


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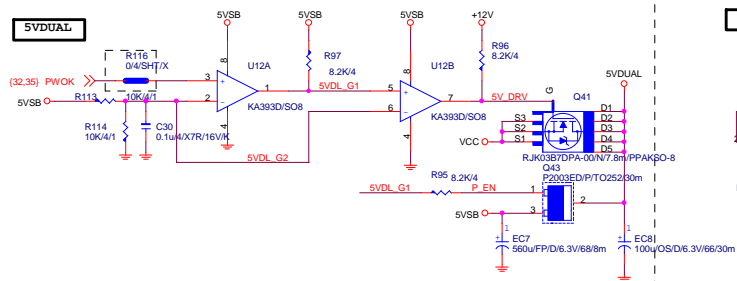


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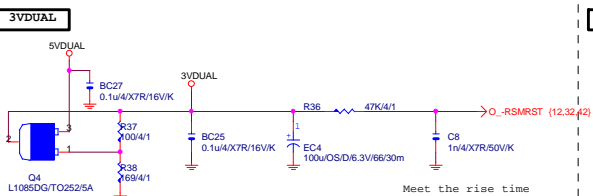
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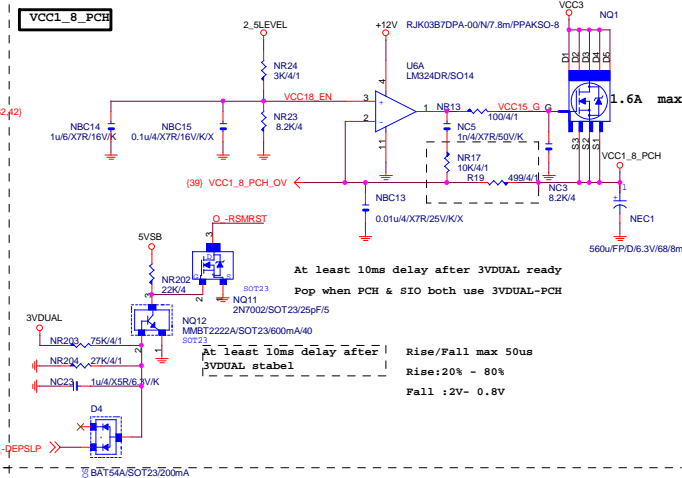
5VDUAL



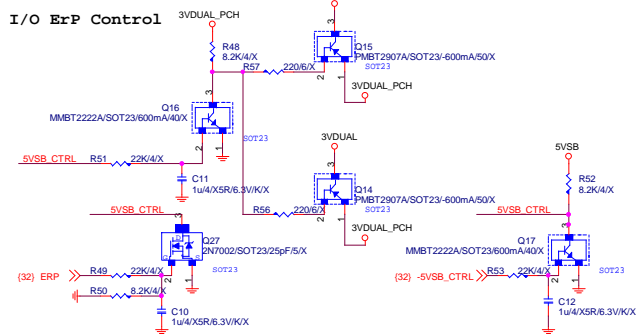
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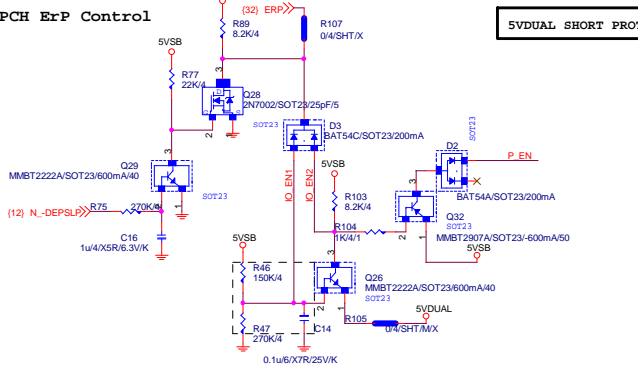
VCC1_8_PCH



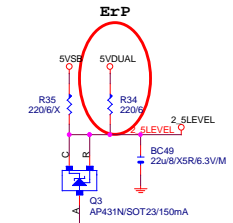
I/O ErP Control



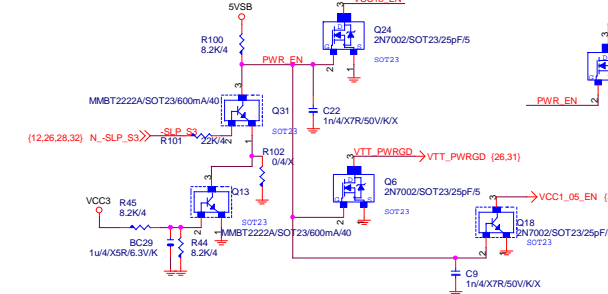
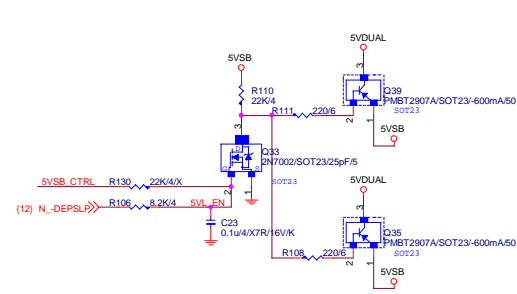
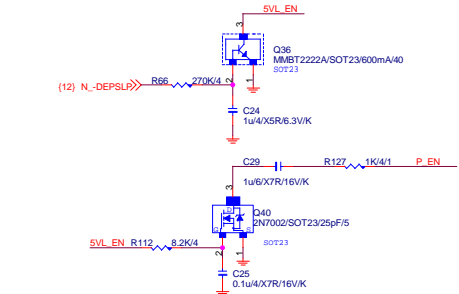
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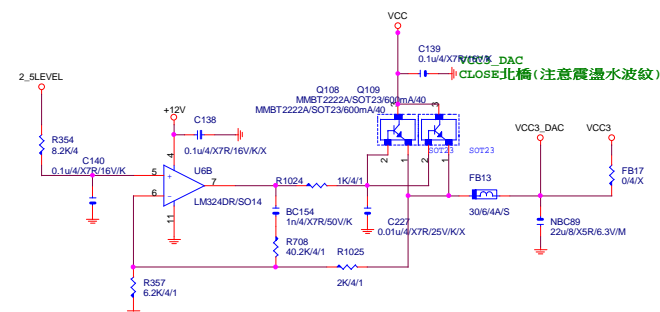
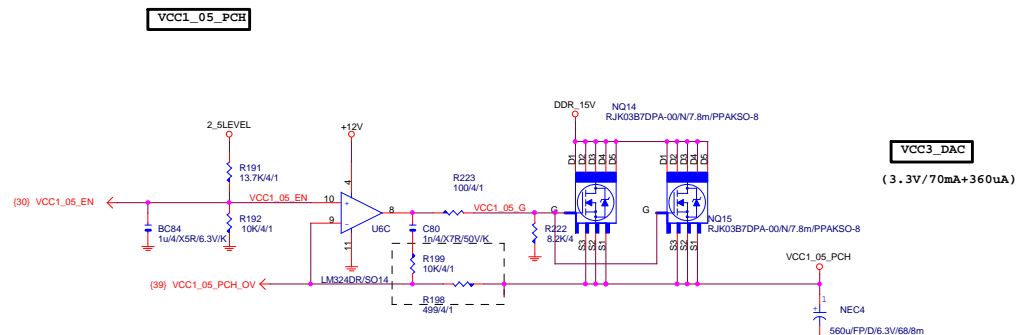


5VDUAL SHORT PROTECT

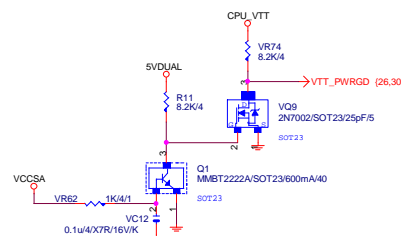
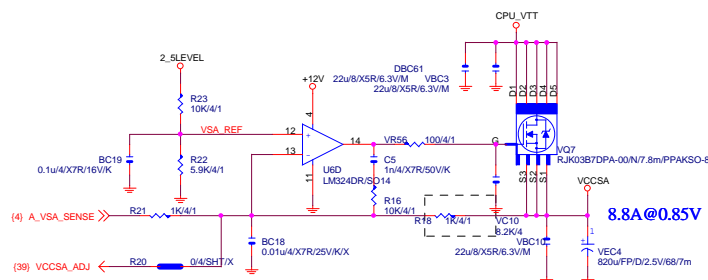
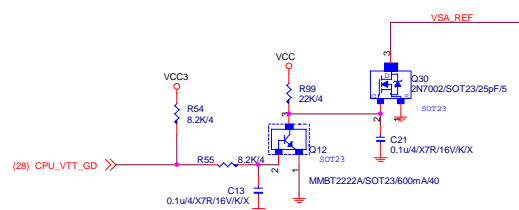


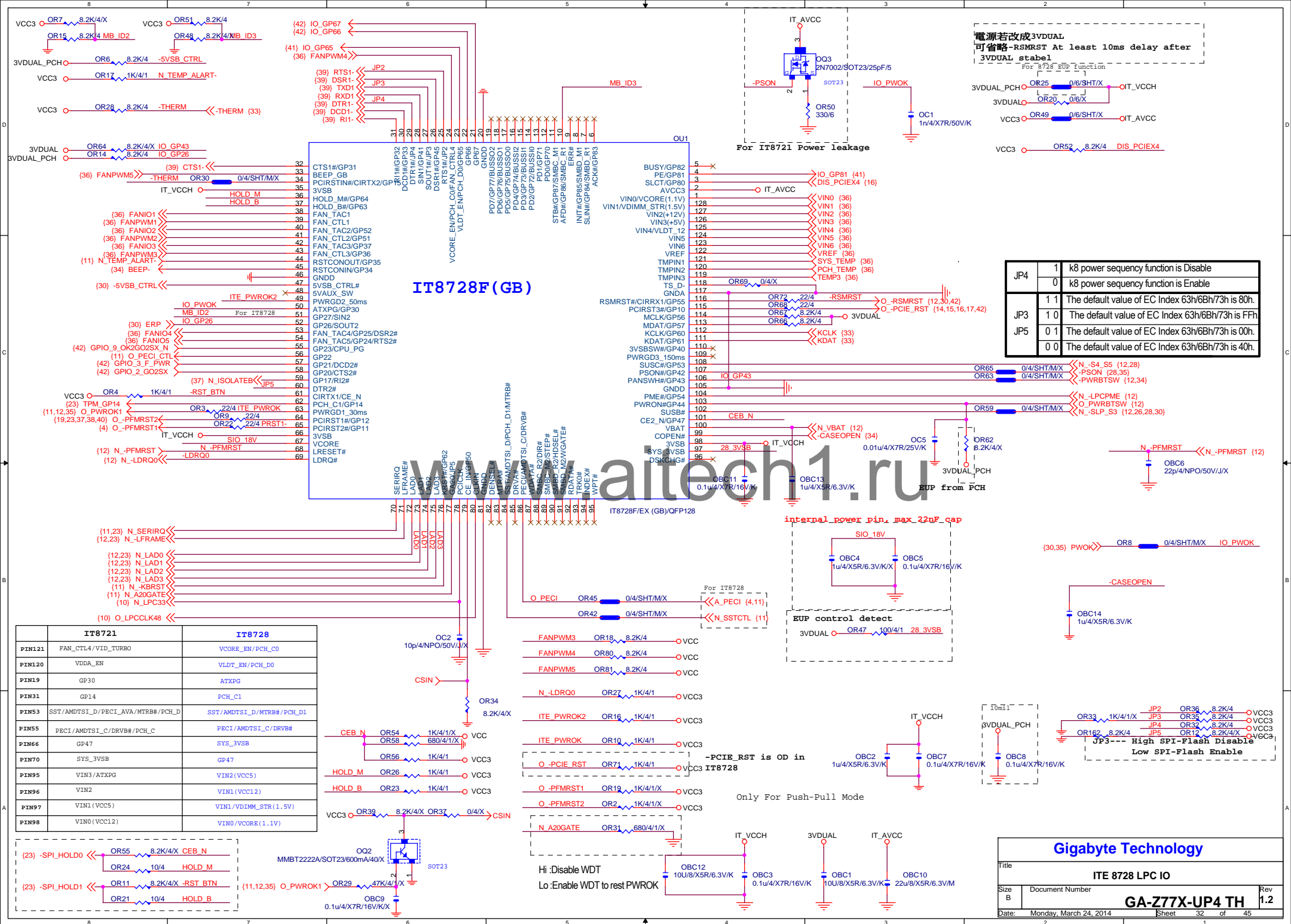
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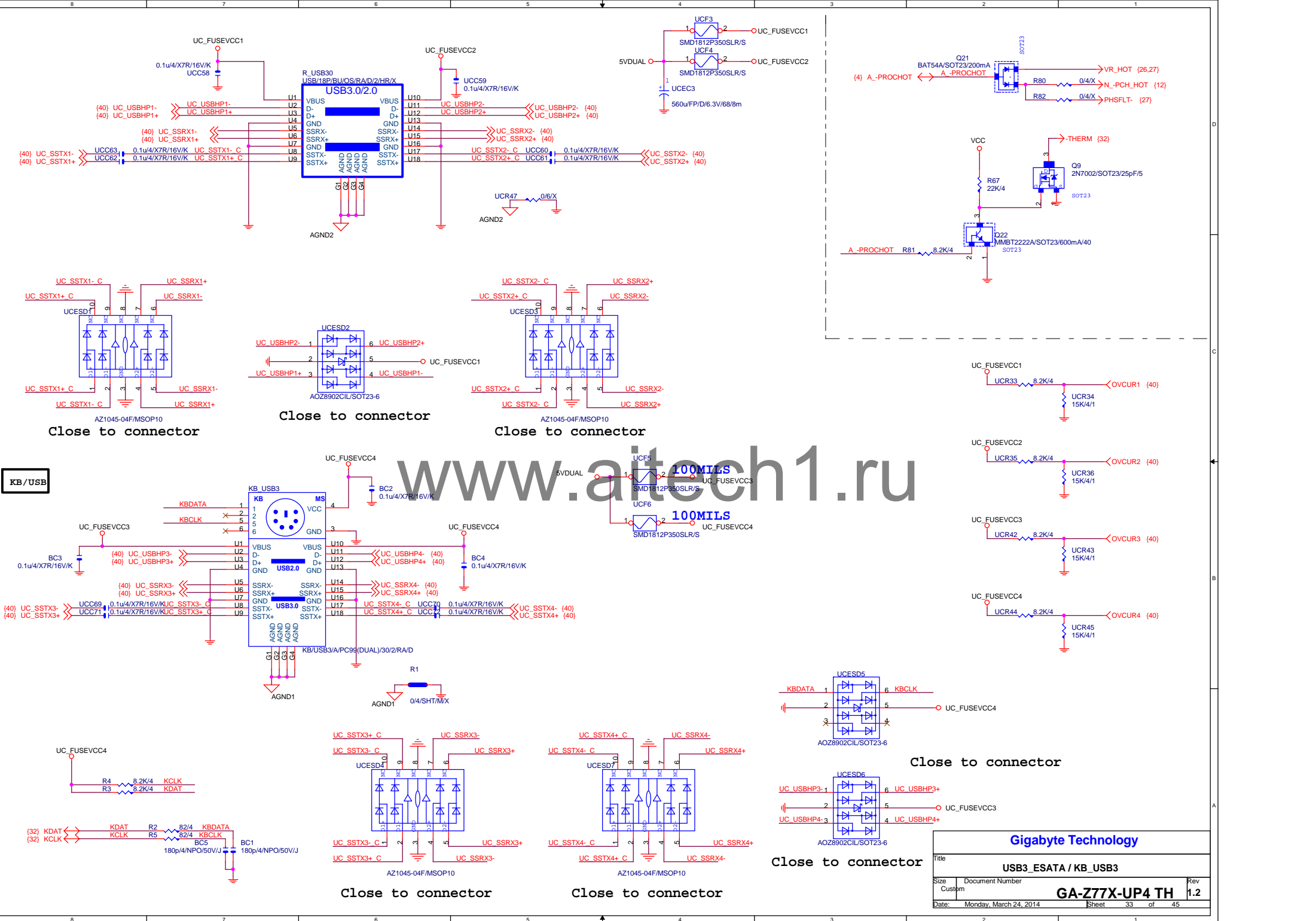




VCC_SA





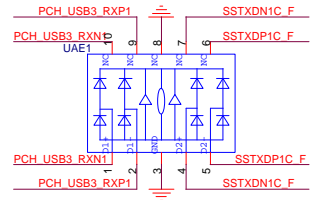
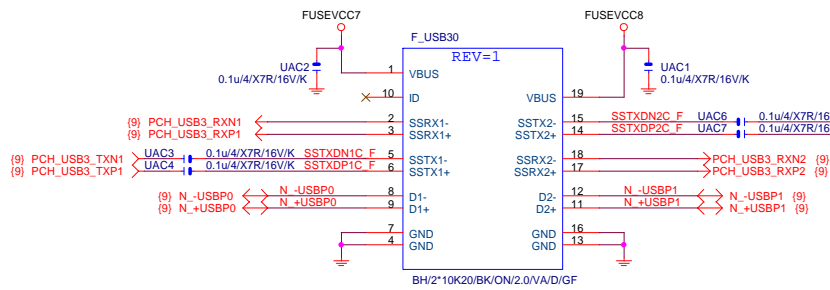


KB/USB

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Gigabyte Technology			
Title USB3_ESATA / KB_USB3			
Size	Document Number	Rev	
Custom		GA-Z77X-UP4 TH 1.2	
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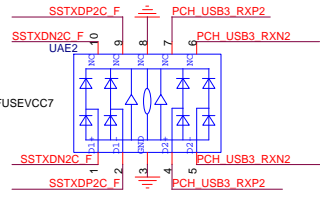
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AZ1045-04F/MSOP10

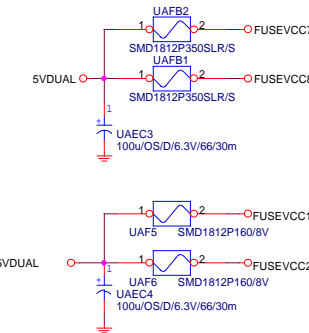
Close to connector

Close to connector

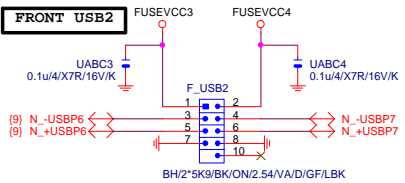
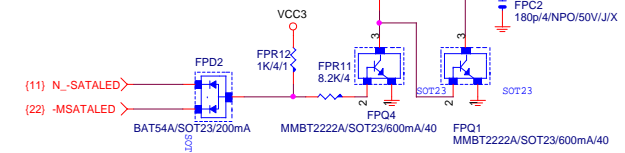


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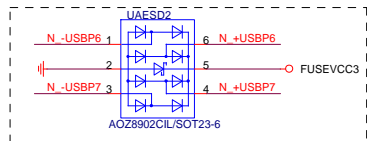
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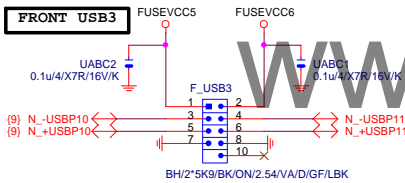
SATA LED



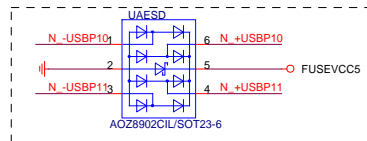
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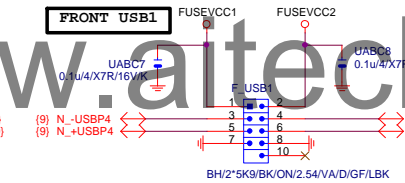
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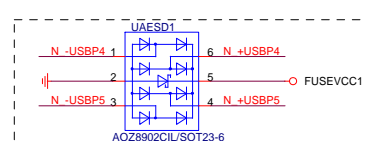
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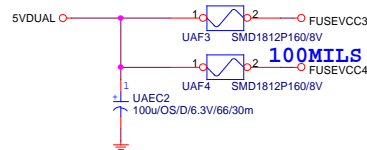
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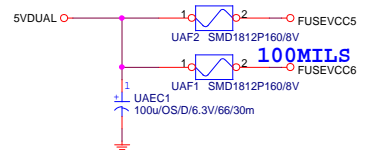
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Close to connector



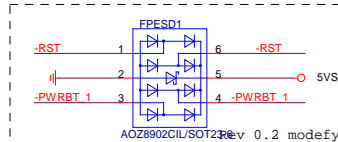
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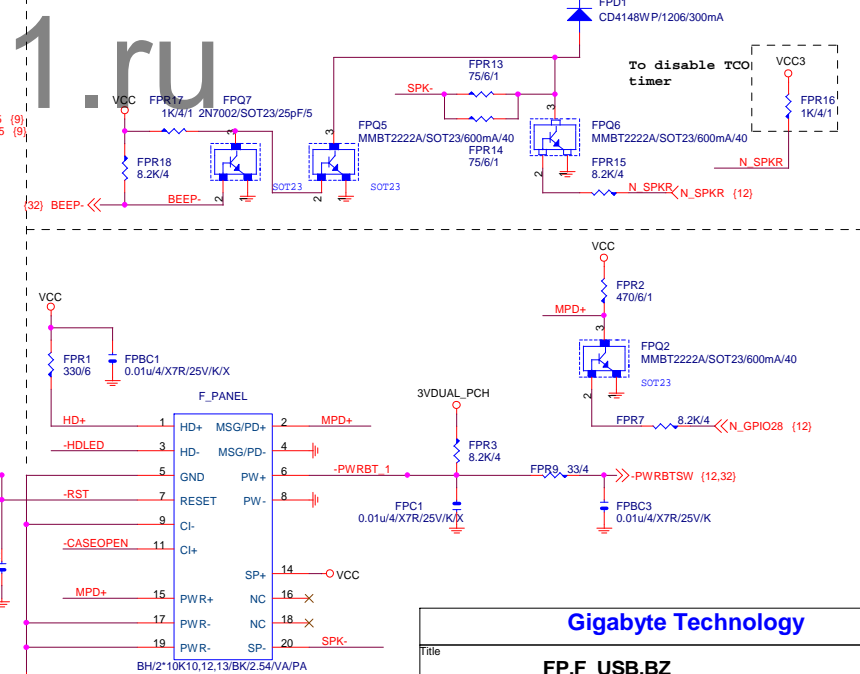
100MILS



INTEL FRONT PANEL



Close to connector

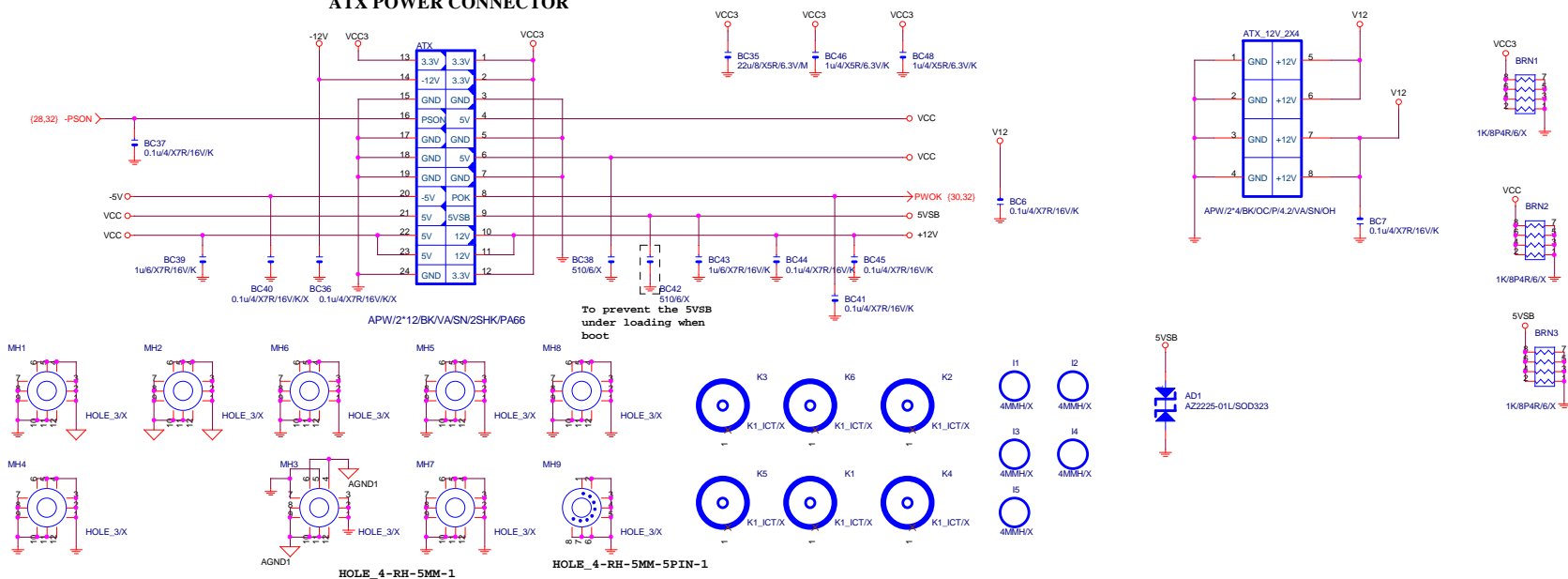


Gigabyte Technology

FF.P_USB.BZ

Size	Document Number	Rev
Custom	GA-Z77X-UP4 TH	1.2

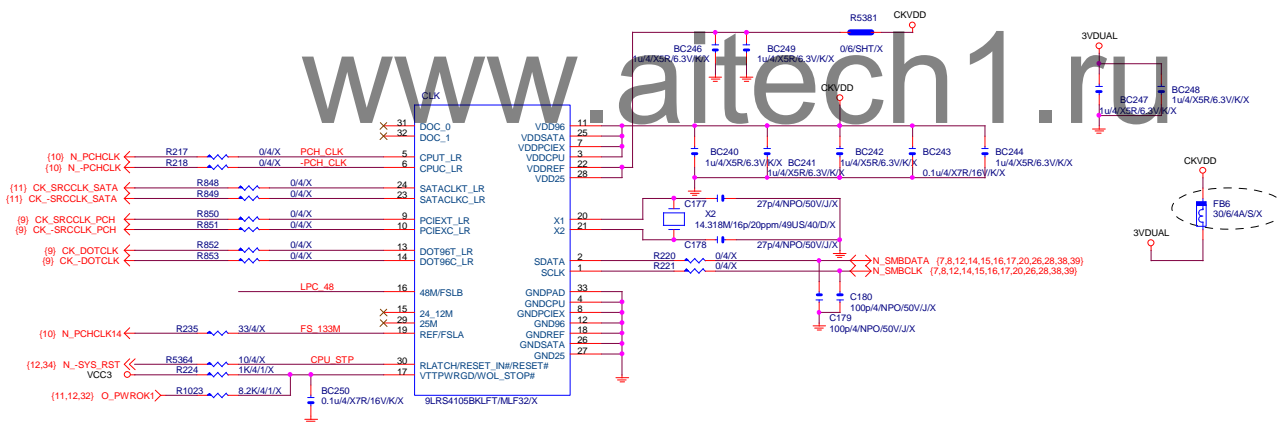
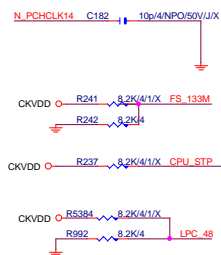
Date: Thursday, February 13, 2014 Sheet 34 of 45



CLK GEN CK505

CPU Frequency Selection

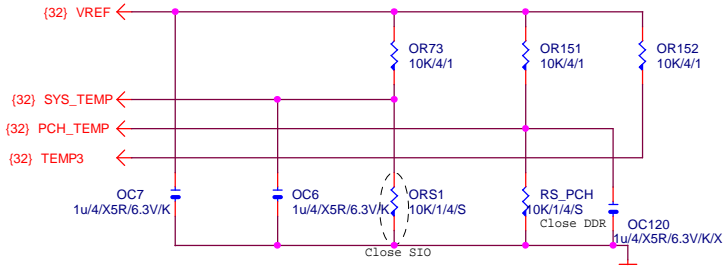
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0	1	133M
1	0	200M
1	1	166M



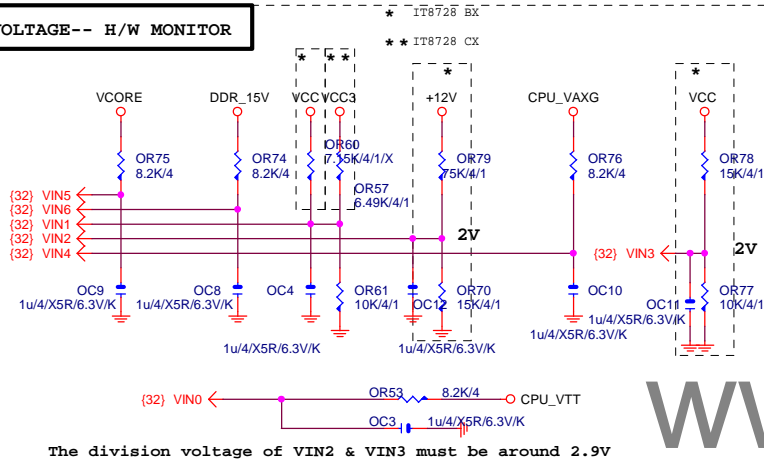
Gigabyte Technology

Title			
ATX POWER CONNECTOR			
Size	Document Number		Rev
Custom	GA-Z77X-UP4 TH		1.2
Date:	Thursday, February 13, 2014	Sheet	35 of 45

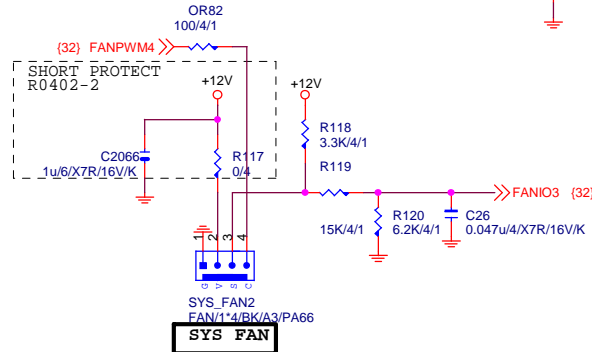
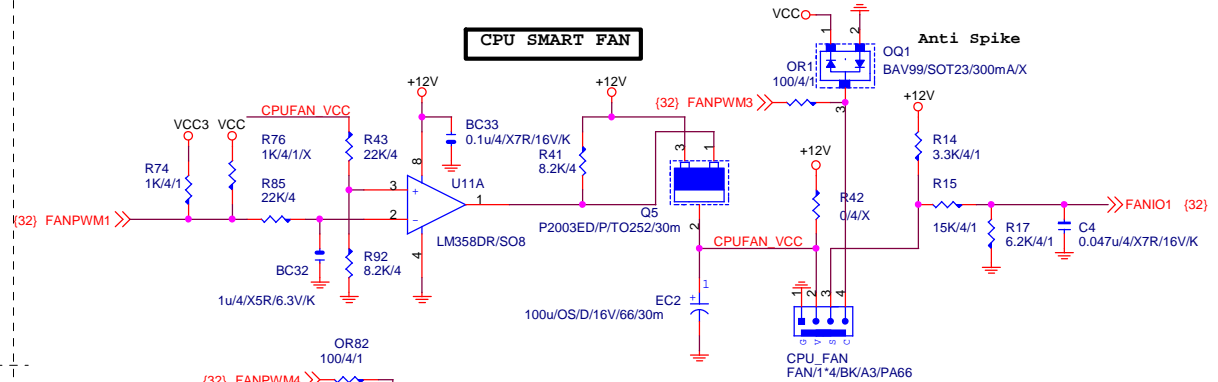
TEMP H/W MONITOR



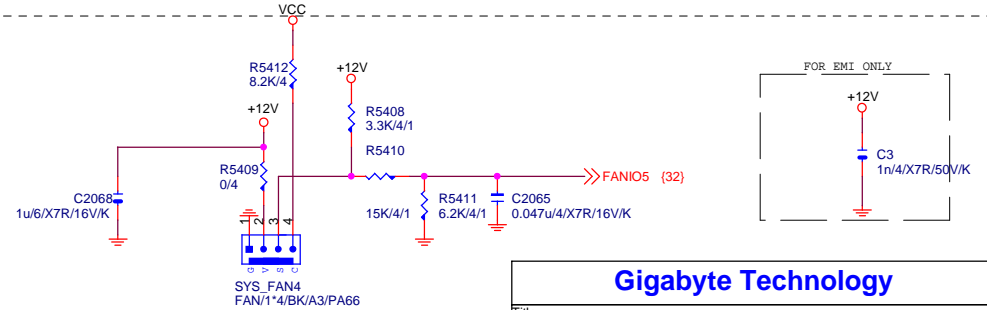
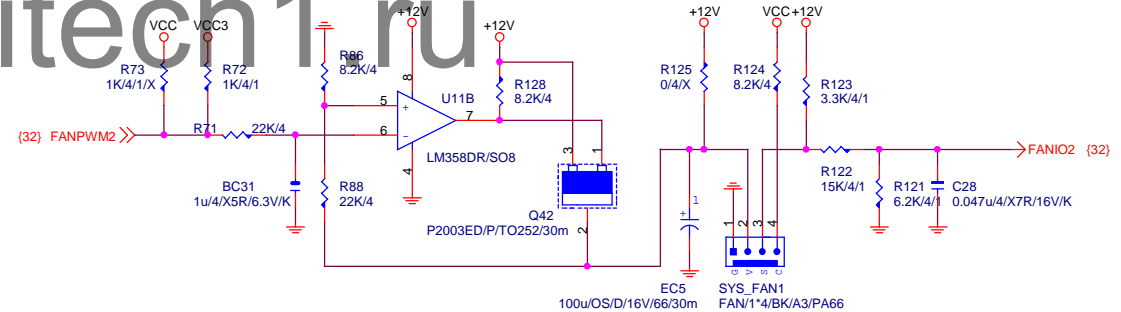
VOLTAGE-- H/W MONITOR



CPU SMART FAN



Linear SYS_FAN

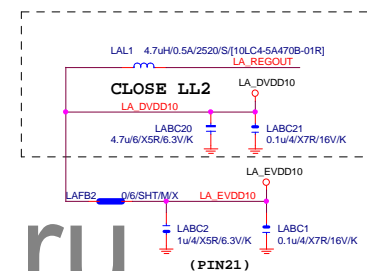
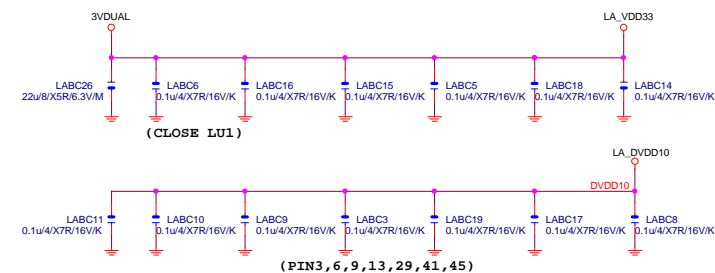
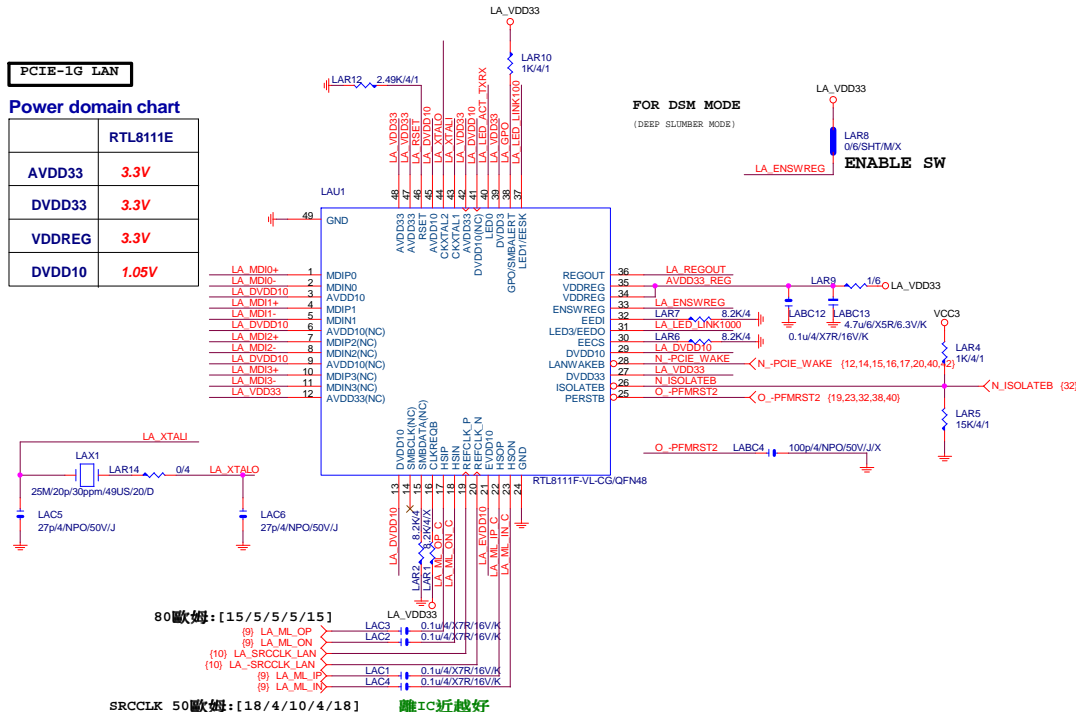


Gigabyte Technology

Title				HWM,KB/MS, FAN CTRL			
Size	Document Number			Rev			
Custom	GA-Z77X-UP4 TH			1.2			
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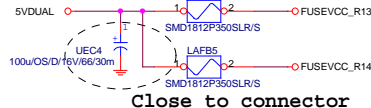
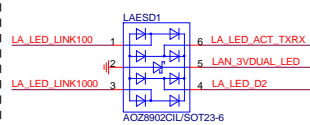
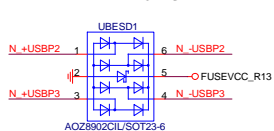
Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



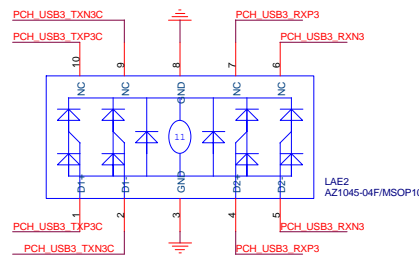
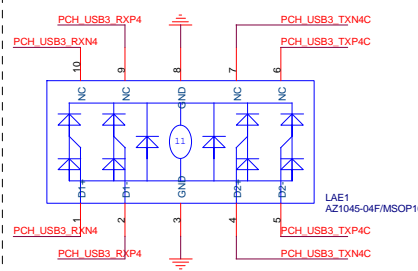
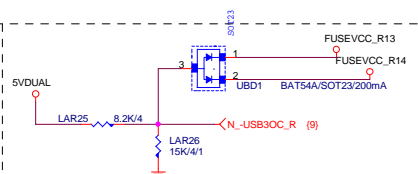
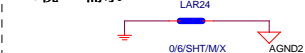
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RMA ESD PROTECT

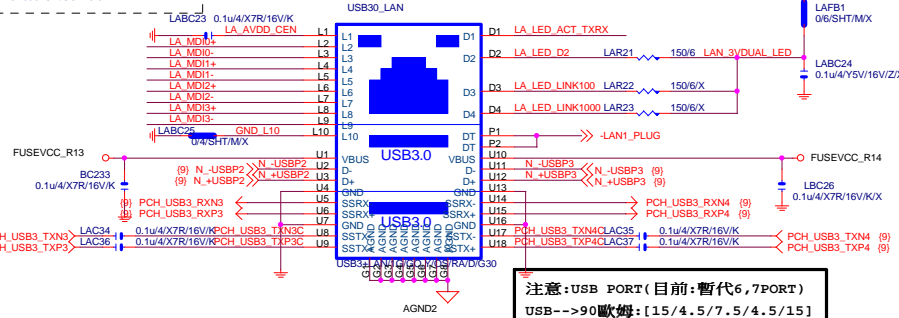


Close to connector

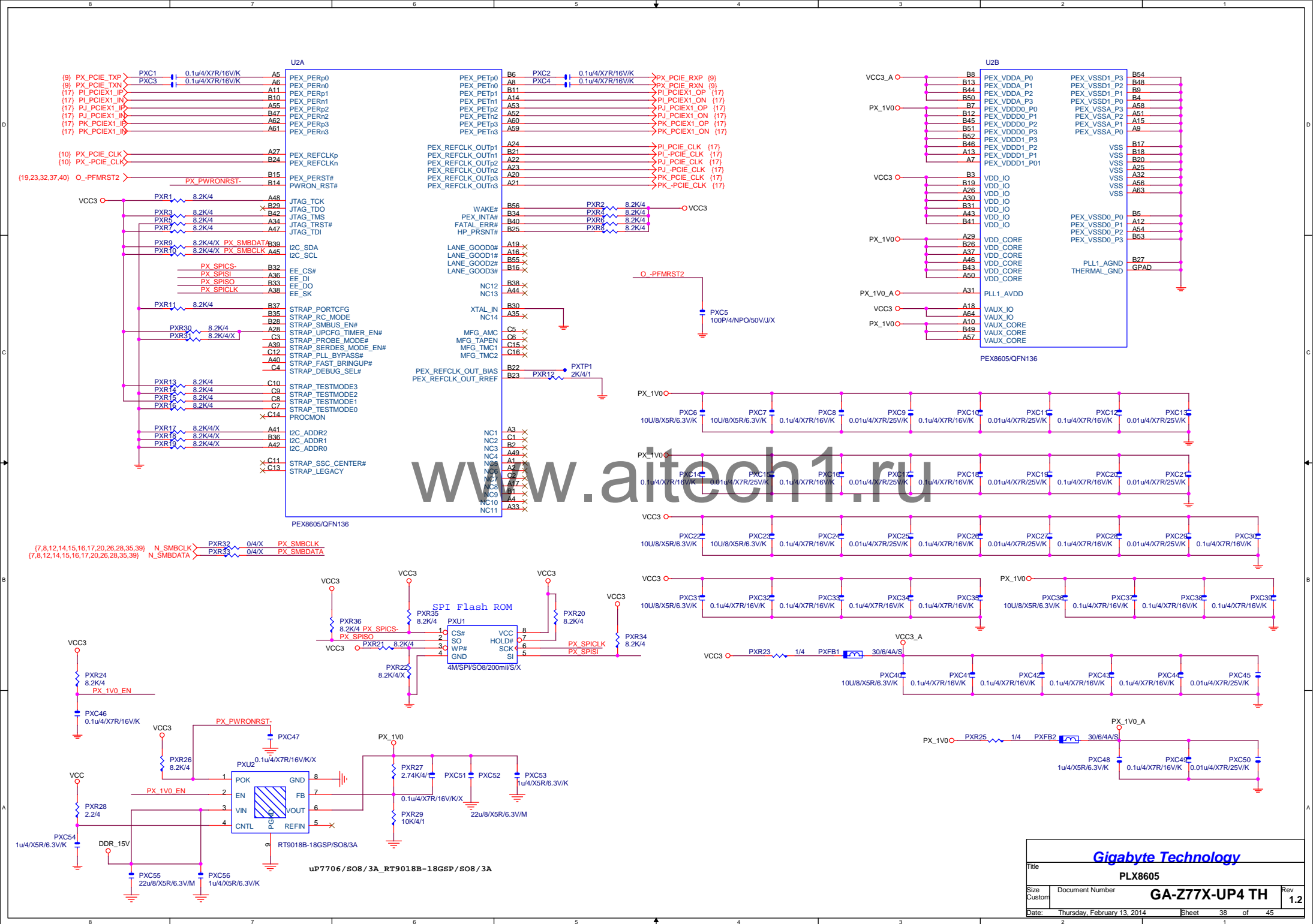
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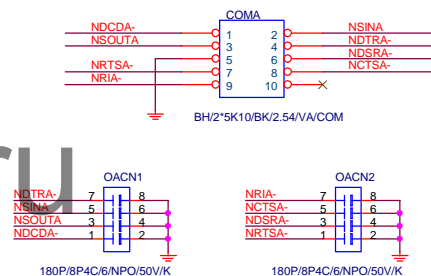
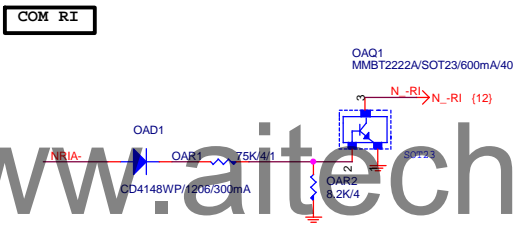
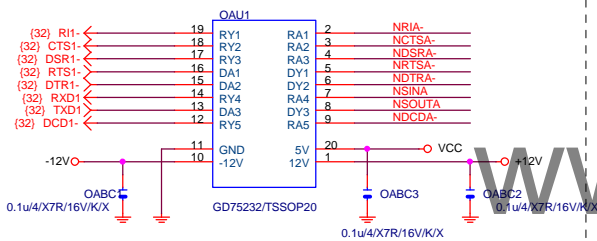
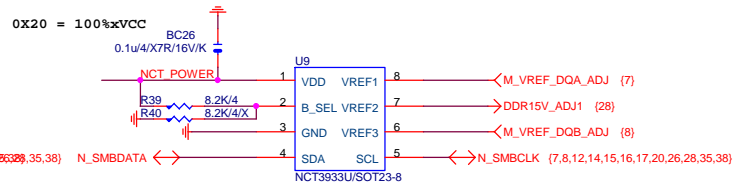
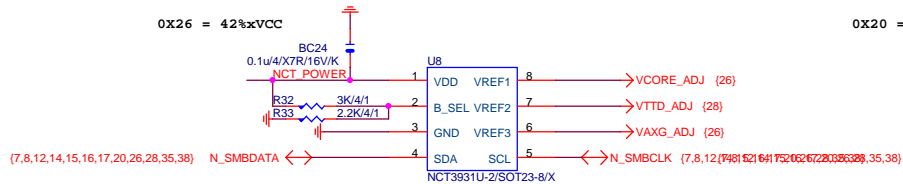
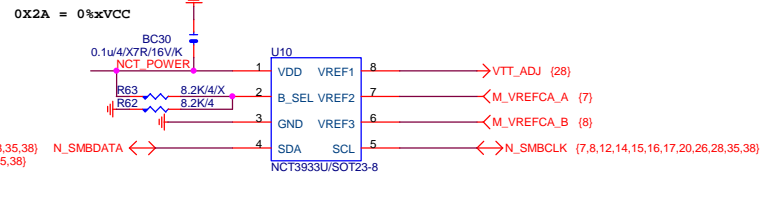
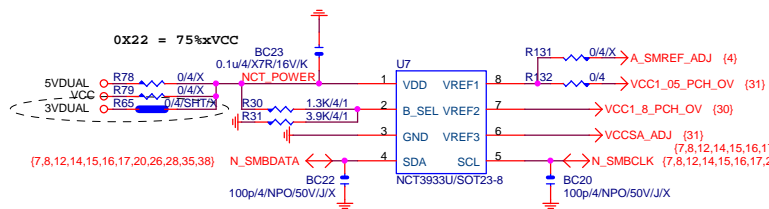


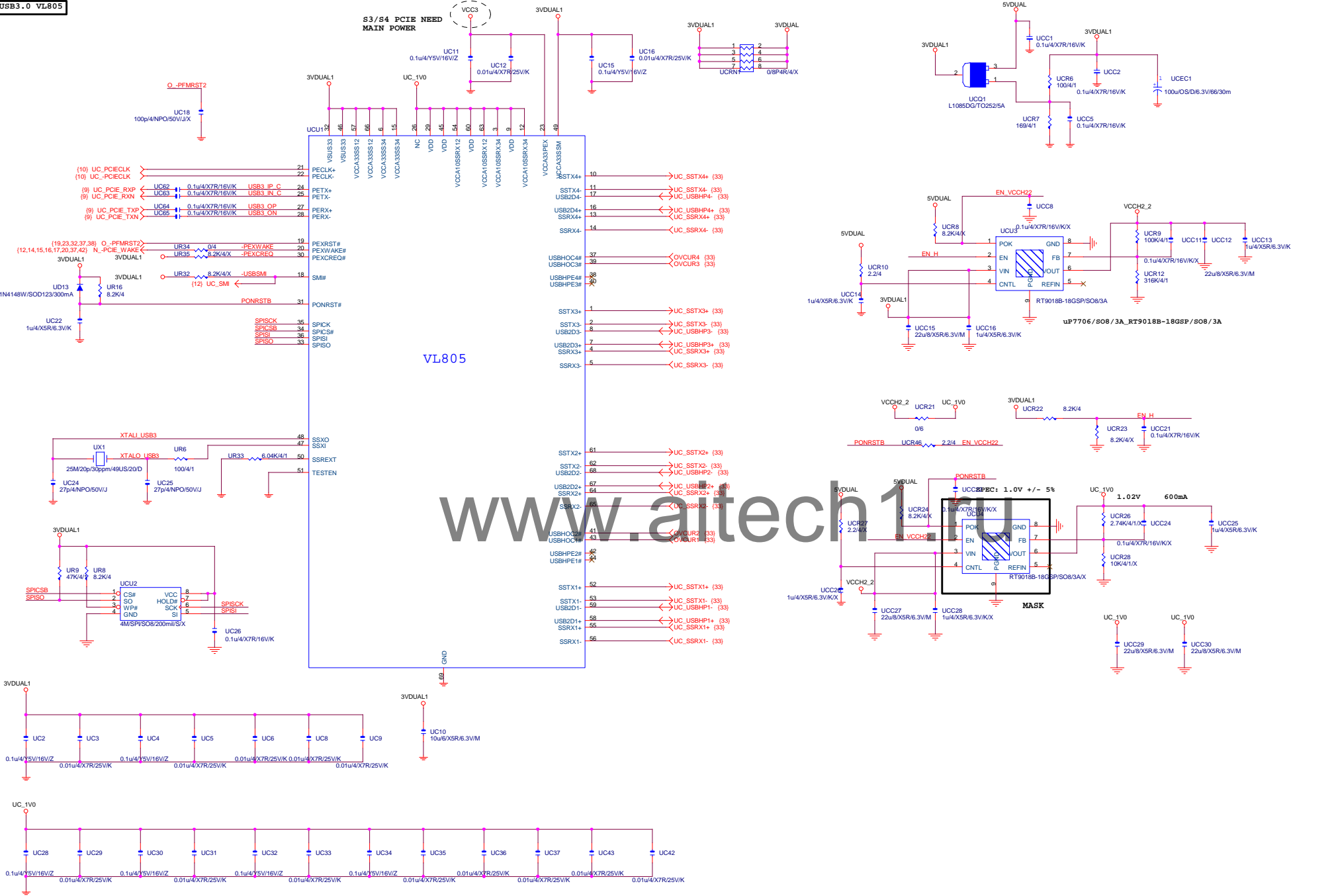
LA MDI-->100歐姐:[20/4/8/4/20]

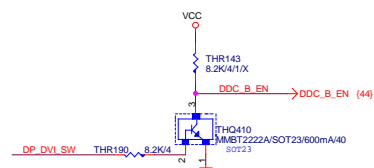
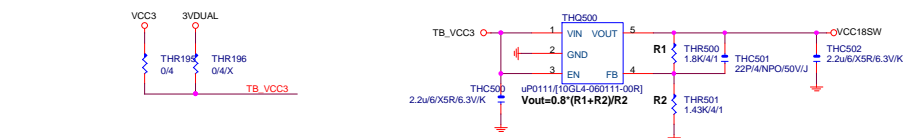
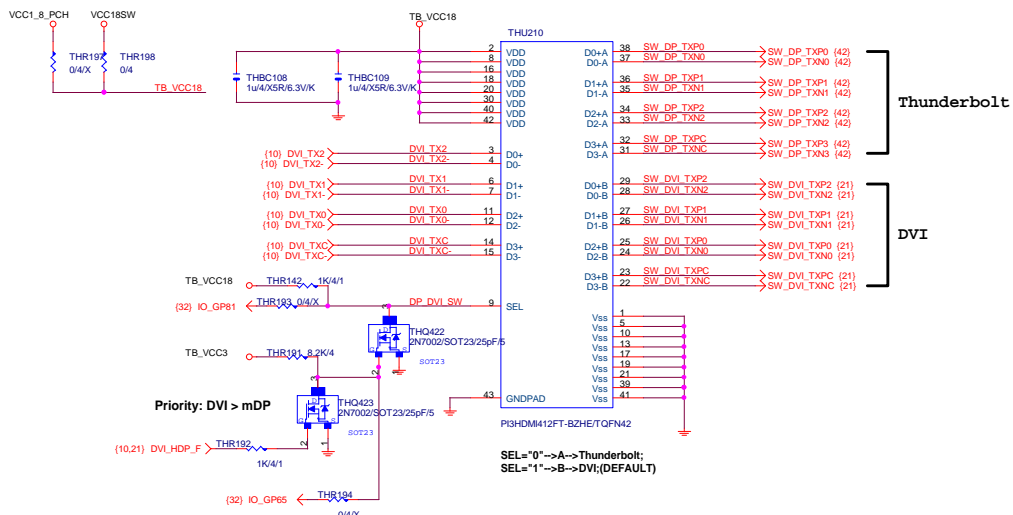


注意:USB PORT(目前:暫代6,7PORT)
USB-->90歐姆:[15/4.5/7.5/4.5/15]



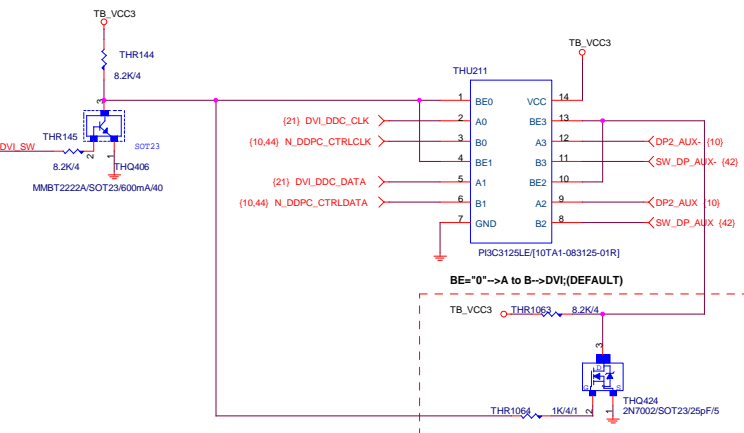






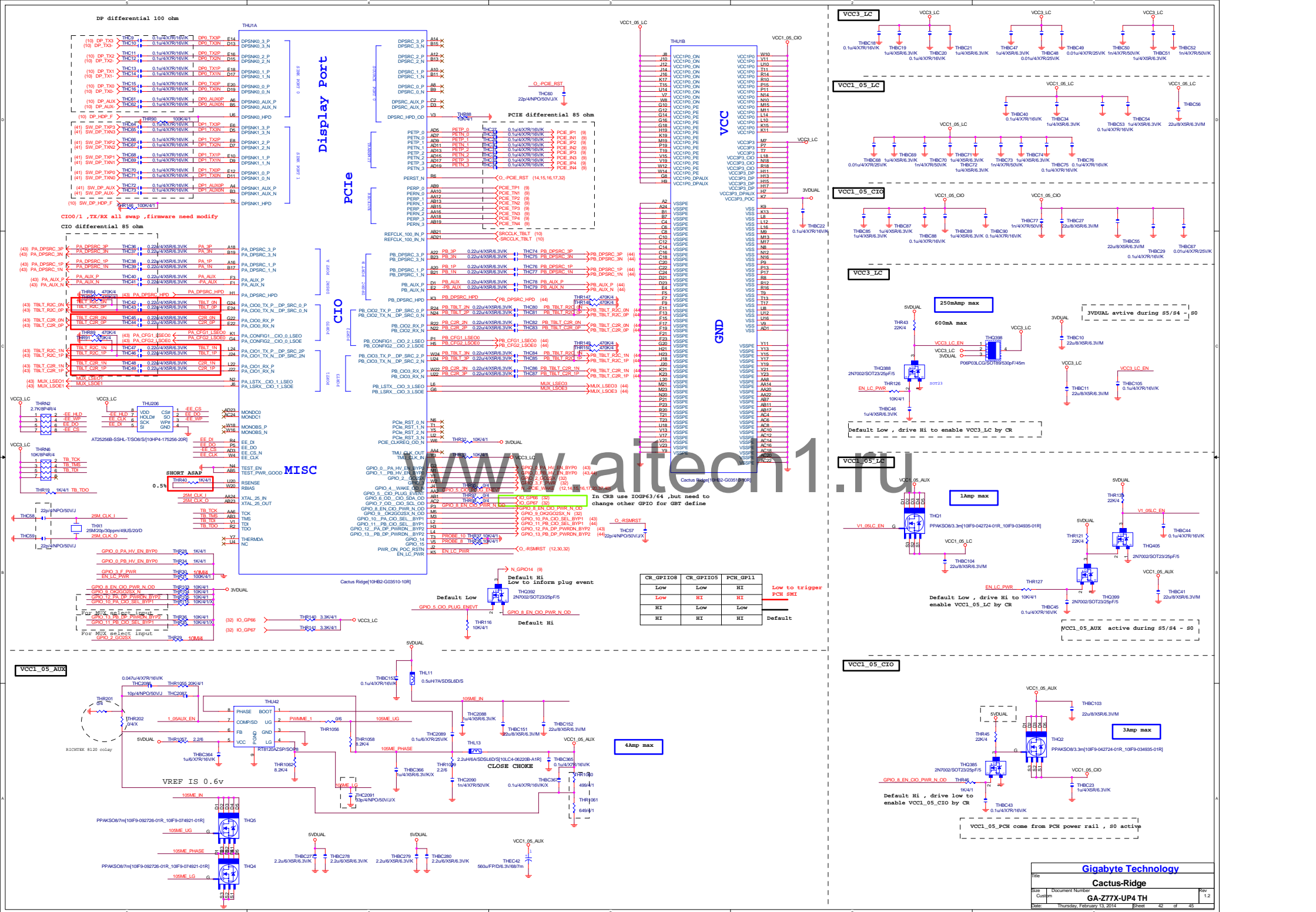
DP_DVI_SW="1"→DDC→PCH to Thunderbolt
DP_DVI_SW="0"→DDC→PCH to DVI(DEFAULT)

DP_DVI_SW="0"→AUX→PCH to Thunderbolt
DP_DVI_SW="1"→AUX→OPEN

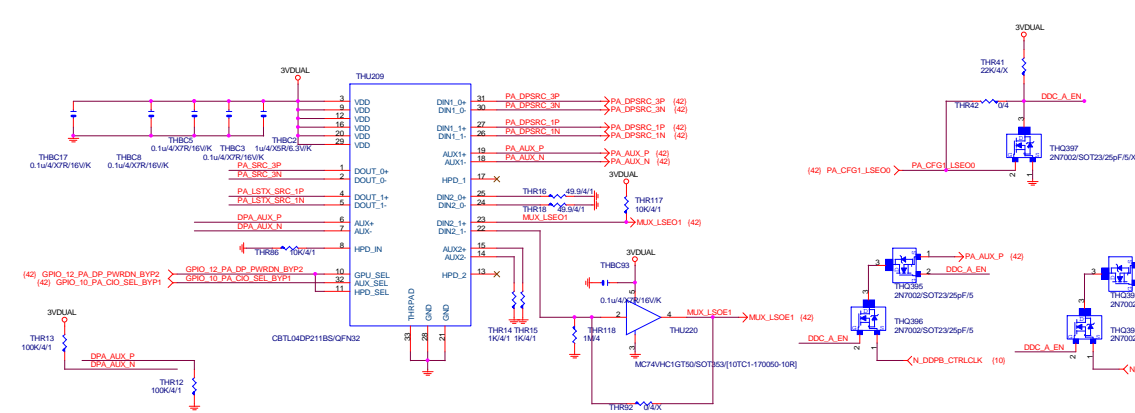


BE="0"→A to B→DVI(DEFAULT)

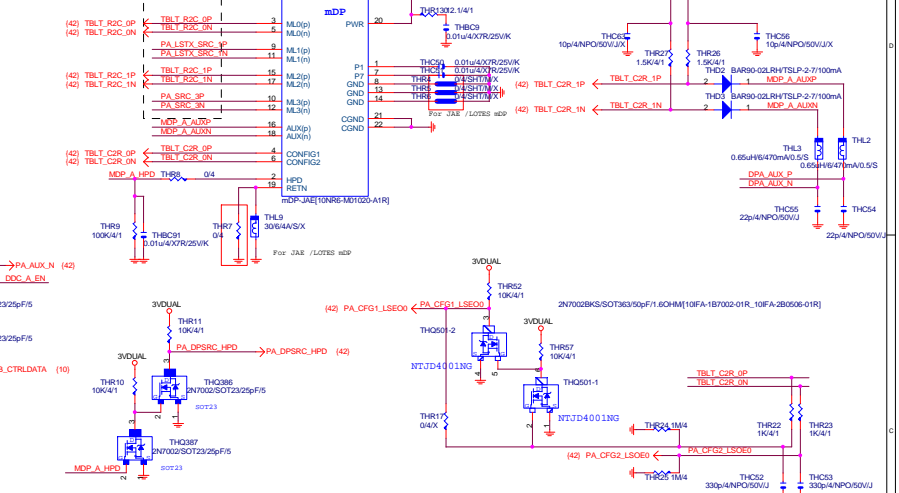
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DP_A

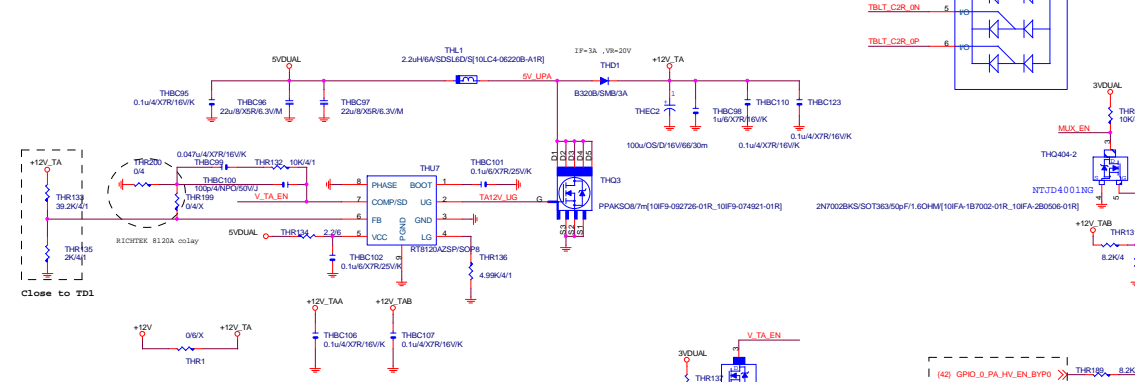


100 speed ,take care layout under 2000mil in whole length

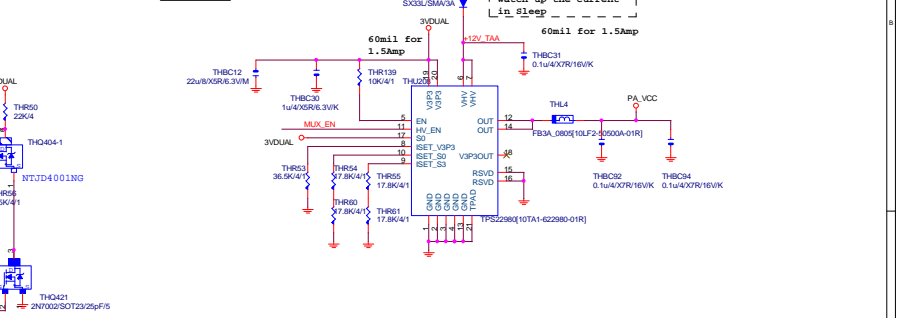


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12V_TB



MDP_POWER



Power Rail	Current budget	S4/S5	S3	S0
VCC3P3_POC	100mA	ON	ON	ON
VCC3_IC	600mA	OFF	ON	ON
VCC1_05_IC	1A	OFF	ON	ON
VCC1_05_CIO	4A	OFF	ON	ON

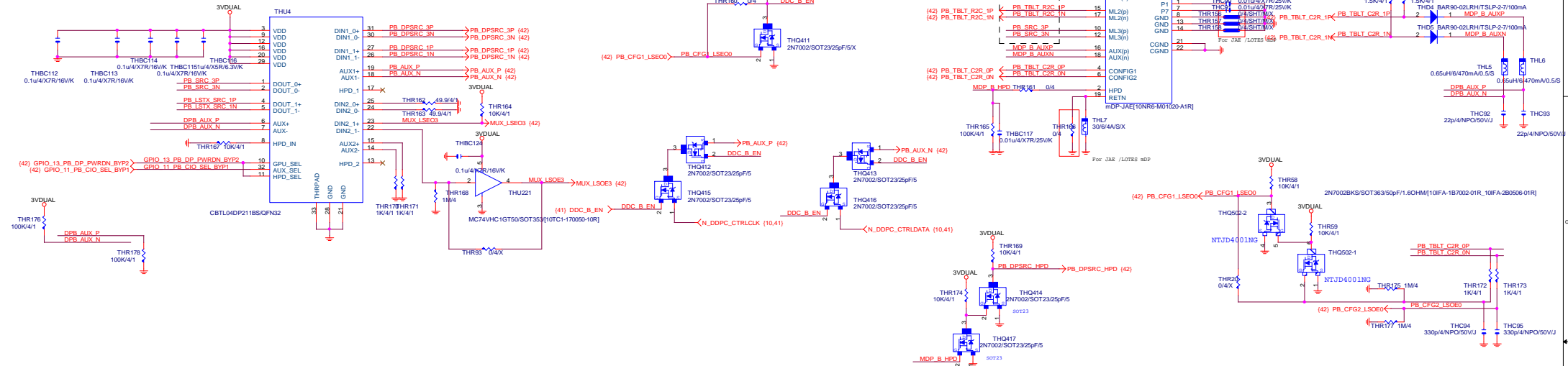
(42) GPIO_0_PA_HV_EN_BYP2
(42.44) GPIO_0_PA_HV_EN_BYP1

PA_VCC	Power level	Current budget
S4/S5	3.3V/12V	150mA
S3	3.3V/12V	150mA
S0	3.3V/12V	1.5A

Take care ! S0 mode always active

EN	RV_EN	OUT
0	0	0V
0	1	0V
1	0	V3P3
1	1	VHV

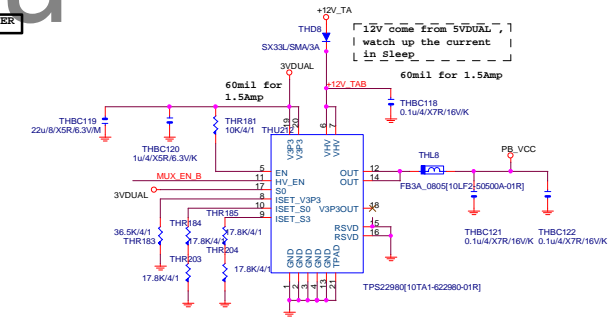
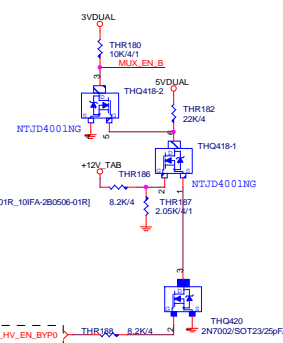
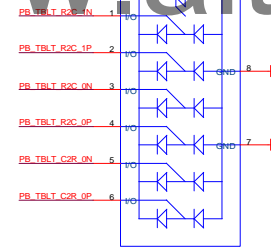
DP_B



Power Sequence
3.3VPOC >> 1.05VLC >> 3.3VLC >> 1.05VCIO

POWER CONSUMPTION	
VCC3P3_POC	10mA
VCC3V3_LC	100mA
VCC1V05_LC	2A
VCC1V05_CIO	1.4A

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PA_VCC	Power level	Current budget
S4/S5	3.3V/12V	150mA
S3	3.3V/12V	150mA
S0	3.3V/12V	1.5A

Take care! S0 mode always active

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